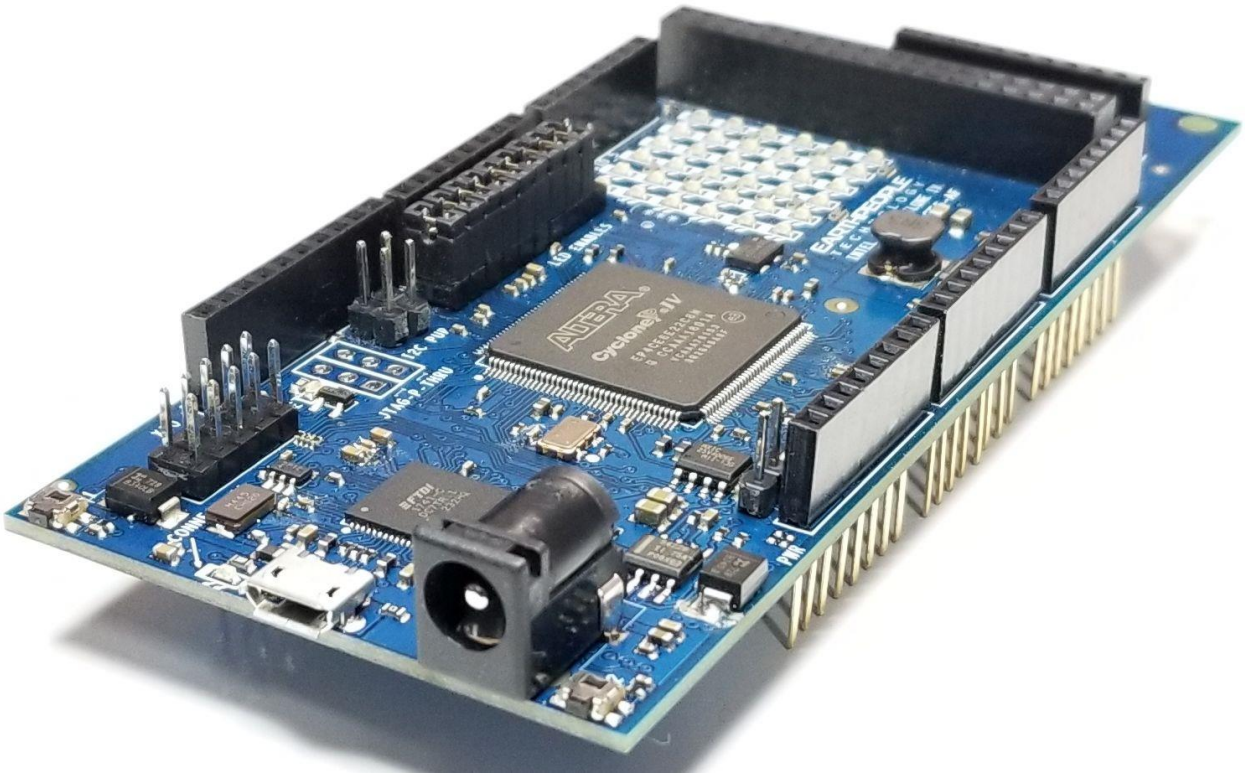
EPT 4CE6-AF-D2

FPGA DEVELOPMENT SYSTEM FOR THE ARDUINO DPL

Data Sheet



The EPT-4CE6-AF-D2 is a part of the EPT USB/FPGA development system. It provides an innovative method of developing and debugging the users microcontroller code. It can also provide a high speed data transfer mechanism between microcontroller and Host PC.

The EPT-4CE6-AF-D2 board is equipped with an Altera EP4CE6E22 FPGA; which is programmed using the Altera Quartus II software. The FPGA has 6,272 Logic Elements along with 276Kbits of RAM. An on board 66 MHz oscillator is used by the EPT-Active-Transfer-Library to provide data transfer rates of 8 Mega Bytes per second. The EPT-Active-Transfer-Library provides control communication between the objective device and the FPGA. Data transfer during the objective device checkout between the PC and the FPGA program is available

via the ActiveHost. The board also includes the following parts.

- Altera EP4CE6E22 FPGA in the TQFP 144 pin package
- 66 MHz oscillator for driving USB data transfers and users code
- 100 MHz oscillator for user clocking
- 63 user Input/Outputs
- Four Green LED's accessible by the user
- Two PCB switches accessible by the user
- All connectors to stack into the Arduino DPL
- FPGA Configuration using the FT2232H Chip.
- Bi-Directional High Speed Data Transfer over USB.

1 Block Diagram

Figure 1 EPT-4CE6-AF Component Location

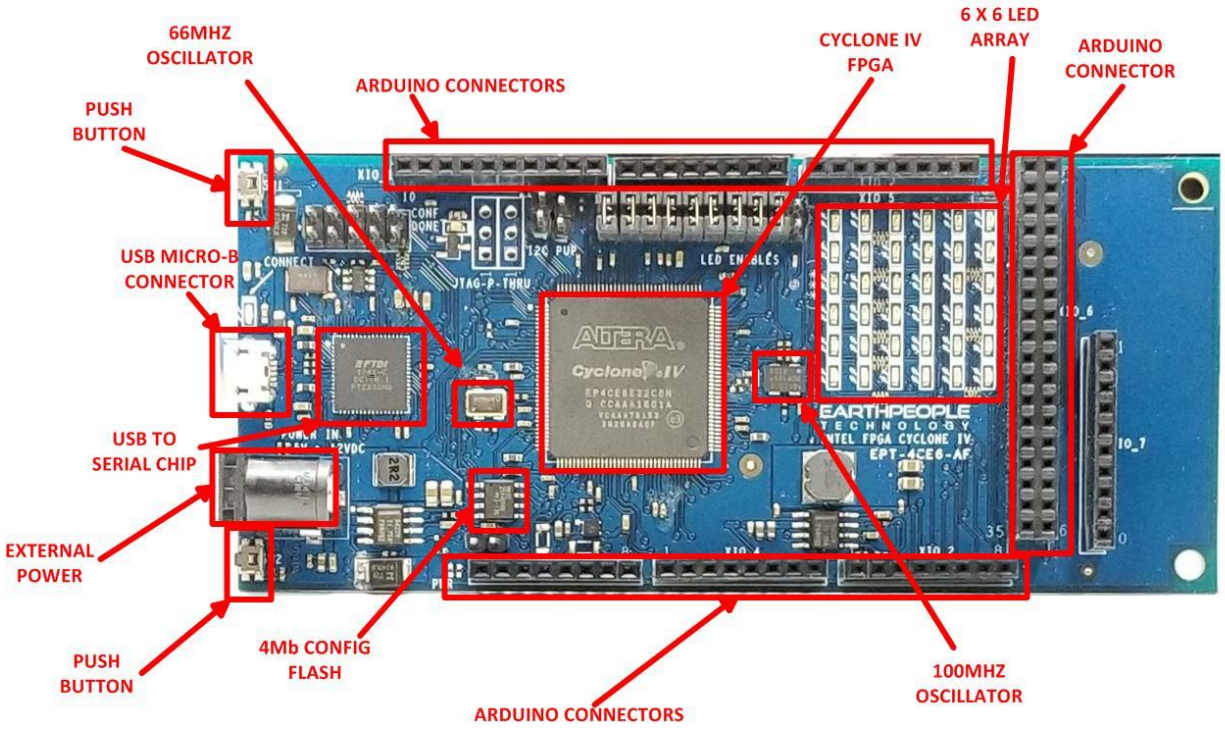
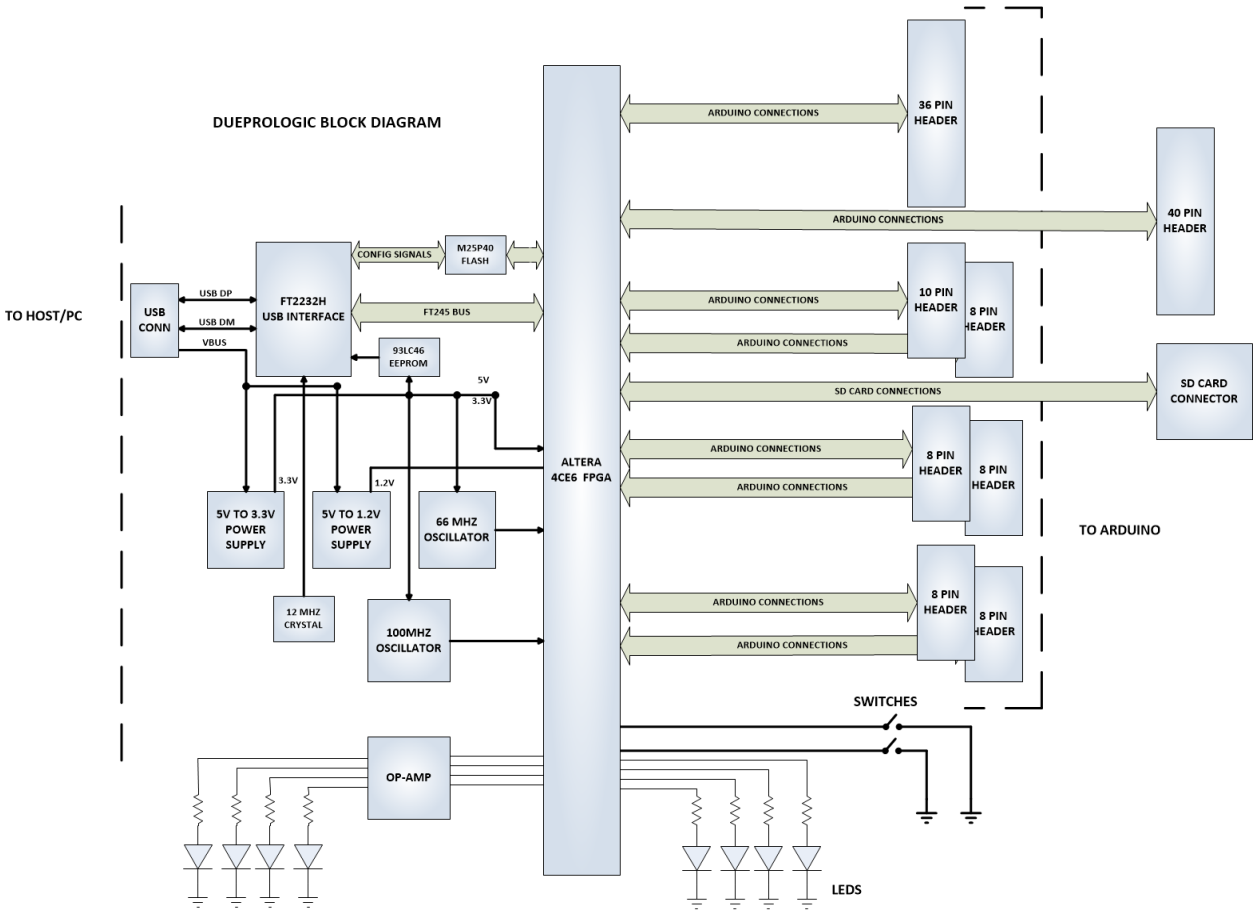


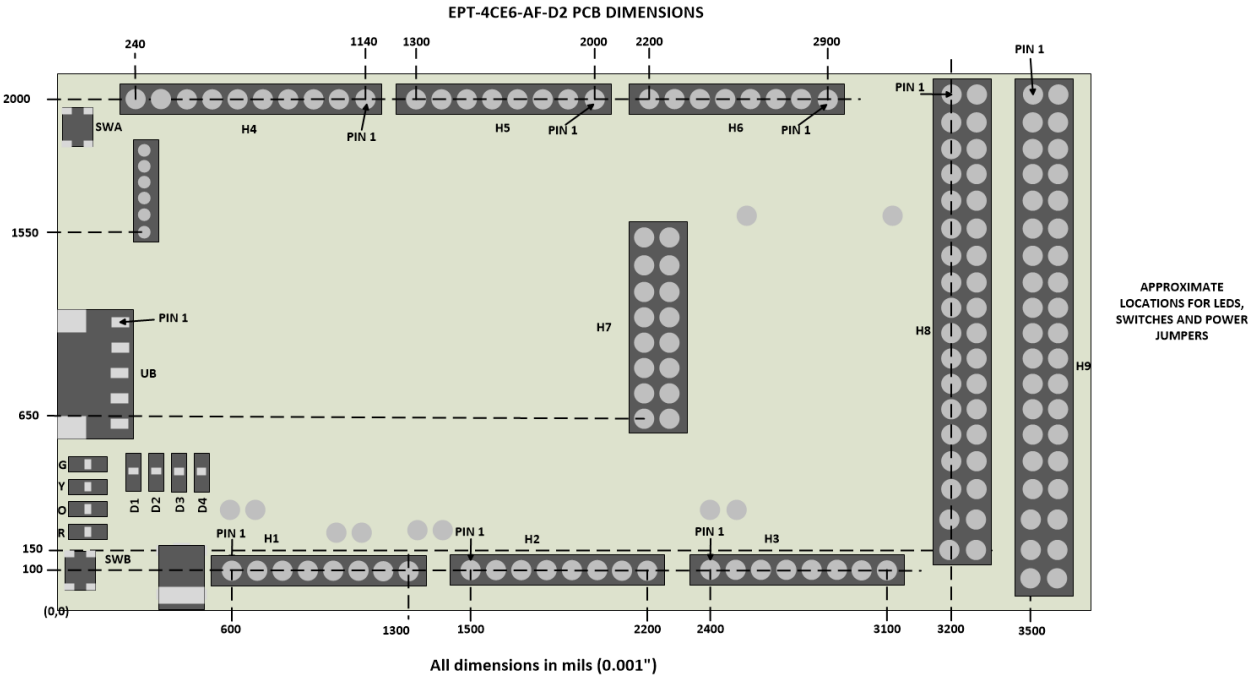
Figure 2 EPT-4CE6-AF Block Diagram



The user's microcontroller code is developed to perform particular functions required by the user. The code is downloaded to the device using the hardware/software system provided as part of the microcontroller development system. The EPT-570-AP USB/FPGA Development System consists of a board base onto which is plugged the FT2232H board. These boards comprise the hardware components of the EPT USB/FPGA development system. The FPGA allows users to write HDL code that will implement any digital logic circuit. The users HDL code is compiled and synthesized and packaged into a programming file. The packaged file is programmed into the FPGA using the side A channel of the USB to Serial chip, FT2232H. The Active_Host DLL is designed to transfer data from the FPGA when it becomes available. The data will be stored into local memory of the PC, and an event will be triggered to inform the user code that data is available from the addressed module of the FPGA. This method, from the user code on the PC, makes the data transfer transparent.

2 Mechanical Dimensions

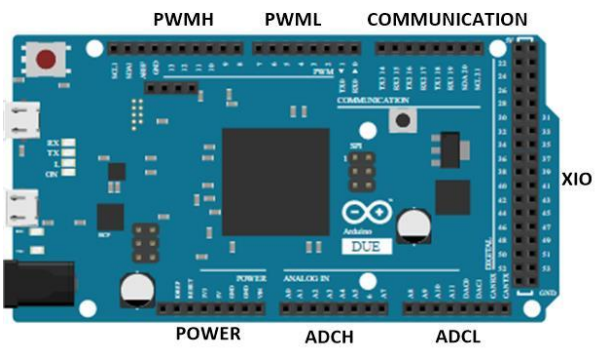
Figure 3 EPT-4CE6-AF Mechanical Dimensions

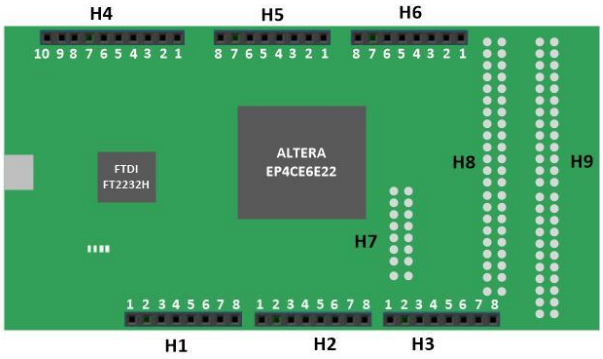


3 Pin Mapping

Figure 4. Pin Mapping between Arduino Due, DueProLogic and FPGA User code

DUE TO DUEPROLOGIC PIN MAPPING





DUE		DUEPROLOGIC			
CONNECTOR	PIN	CONNECTOR	PIN	SIGNAL	FPGA I/O
PWMH	TWCK0	H4	10	D8	XIO_1[6]
	TWD0		9	D9	XIO_1[7]
	AREF		8	D10	XIO_2[0]
			7	D11	XIO_2[1]
	13		6	D12	XIO_2[2]
	12		5	NC	--
	11		4	GND	--
	10		3	NC	--
	9		2	D70	XIO_7[1]
	8		1	D71	XIO_7[2]
PWML	7	H5	8	NC	--
	6		7	NC	--
	5		6	D2	XIO_1[0]
	4		5	D3	XIO_1[1]
	3		4	D4	XIO_1[2]

	2		3	D5	XIO_1[3]
	UTXD		2	D6	XIO_1[4]
	URXD		1	D7	XIO_1[5]
COMMUNICATION	TWCK1	H6	8	NC	--
	TWD1		7	NC	--
	19		6	D19	SD_CMD
	18		5	D18	XIO_2_IN[4]
	17		4	D17	XIO_2_IN[3]
	16		3	D16	XIO_2_IN[2]
	15		2	D15	XIO_2_IN[1]
	14		1	D14	XIO_2_IN[0]
ADCH	CANTX0	H3	8	D69	XIO_7[0]
	CANTRX0		7	D68	SD_DATA[1]
	DAC1		6	NC	--
	DAC0		5	NC	--
	AD11		4	NC	--
	AD10		3	D64	SD_DATA[1]
	AD9		2	D63	SD_CLK
	AD8		1	D62	SD_DATA[0]
ADCL	AD7	H2	8	NC	--
	AD6		7	NC	--
	AD5		6	NC	--
	AD4		5	NC	--
	AD3		4	NC	--
	AD2		3	NC	--
	AD1		2	NC	--
	AD0		1	D54	SD_DATA[2]
SPI	MISO	H7	6	D22	XIO_3[0]
	+5V		5	D62	--
	SPCK		4	D75	XIO_7[4]
	MOSI		3	D76	XIO_7[5]
	RESET		2	D17	--

	GND		1	D74	XIO_7[3]
XIO	GND	H8	36	GND	--
	GND		35	GND	--
	53		34	D53	XIO_6[7]
	52		33	D52	XIO_6[6]
	51		32	D51	XIO_6[5]
	50		31	D50	XIO_6[4]
	49		30	D49	XIO_6[3]
	48		29	D48	XIO_6[2]
	47		28	D47	XIO_6[1]
	46		27	D46	XIO_6[0]
	45		26	D45	XIO_5[7]
	44		25	D44	XIO_5[6]
	43		24	D43	XIO_5[5]
	42		23	D42	XIO_5[4]
	41		22	D41	XIO_5[3]
	40		21	D40	XIO_5[2]
	39		20	D39	XIO_5[1]
	38		19	D38	XIO_5[0]
	37		18	D37	XIO_4[7]
	36		17	D36	XIO_4[6]
	35		16	D35	XIO_4[5]
	34		15	D34	XIO_4[4]
	33		14	D33	XIO_4[3]
	32		13	D32	XIO_4[2]
	31		12	D31	XIO_4[1]
	30		11	D30	XIO_4[0]
	29		10	D29	XIO_3[7]
	28		9	D28	XIO_3[6]
	27		8	D27	XIO_3[5]
	26		7	D26	XIO_3[4]
	25		6	D25	XIO_3[3]
	24		5	D24	XIO_3[2]
	23		4	D23	XIO_3[1]
	22		3	D22	XIO_3[0]

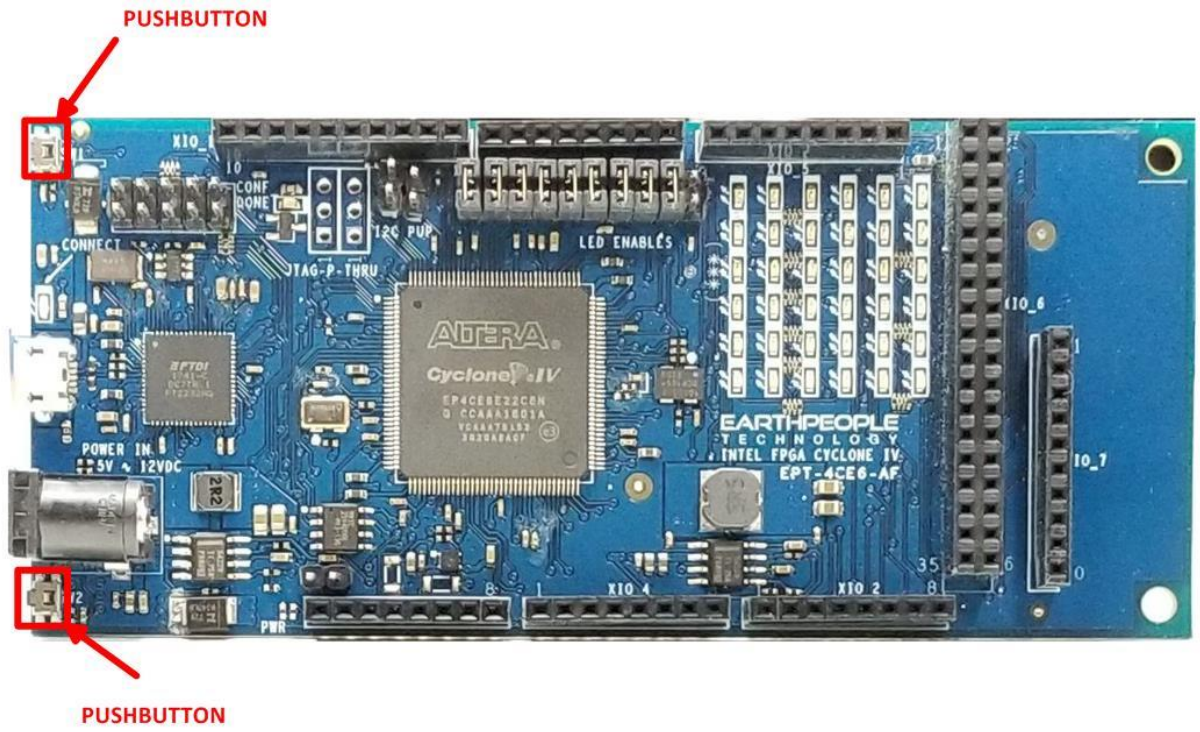
	+5V		2	+5V	--
	+5V		1	+5V	--
--	--	H9	40	+3.3V	--
			39	+3.3V	--
			38	GND	--
			37	GND	--
			36	ULR	ULR
			35	ULO	ULO
			34	ULY	ULY
			33	ULG	ULG
			32	D51	XIO_6[5]
			31	D53	XIO_6[7]
			30	D50	XIO_6[4]
			29	D52	XIO_6[6]
			28	D49	XIO_6[3]
			27	D45	XIO_5[7]
			26	D48	XIO_6[2]
			25	D44	XIO_5[6]
			24	D47	XIO_6[1]
			23	D43	XIO_5[5]
			22	D46	XIO_6[0]
			21	D42	XIO_5[4]
			20	D33	XIO_4[3]
			19	D41	XIO_5[3]
			18	D32	XIO_4[2]
			17	D40	XIO_5[2]
			16	D31	XIO_4[1]
			15	D39	XIO_5[1]
			14	D30	XIO_4[0]
			13	D38	XIO_5[0]
			12	D28	XIO_3[6]
			11	D37	XIO_4[7]
			10	D27	XIO_3[5]
			9	D36	XIO_4[6]
			8	D26	XIO_3[4]

			7	D35	XIO_4[5]
			6	D25	XIO_3[3]
			5	D34	XIO_4[4]
			4	D24	XIO_3[2]
			3	D29	XIO_3[7]
			2	D23	XIO_3[1]
			1	D22	XIO_3[0]
--	--	MICRO-SD	12	GND	--
			11	GND	--
			10	GND	--
			9	GND	--
			8	D54	SD_DATA[2]
			7	D64	SD_DATA[3]
			6	D19	SD_CMD
			5	GND	--
			4	GND	--
			3	D63	SD_CLK
			2	D62	SD_DATA[0]
			1	D68	SD_DATA[1]

4 Pushbutton switches

There are two pushbutton switches on the DueProLogic. Both are momentary contact switches. They include a 1uF cap to ground to debounce both switches.

Component	**Net Name**	**Pin on FPGA**	**Signal in EPT Project Pinout**	
SW1	UB66	25	UBA	
SW2	UB67	24	UBB	



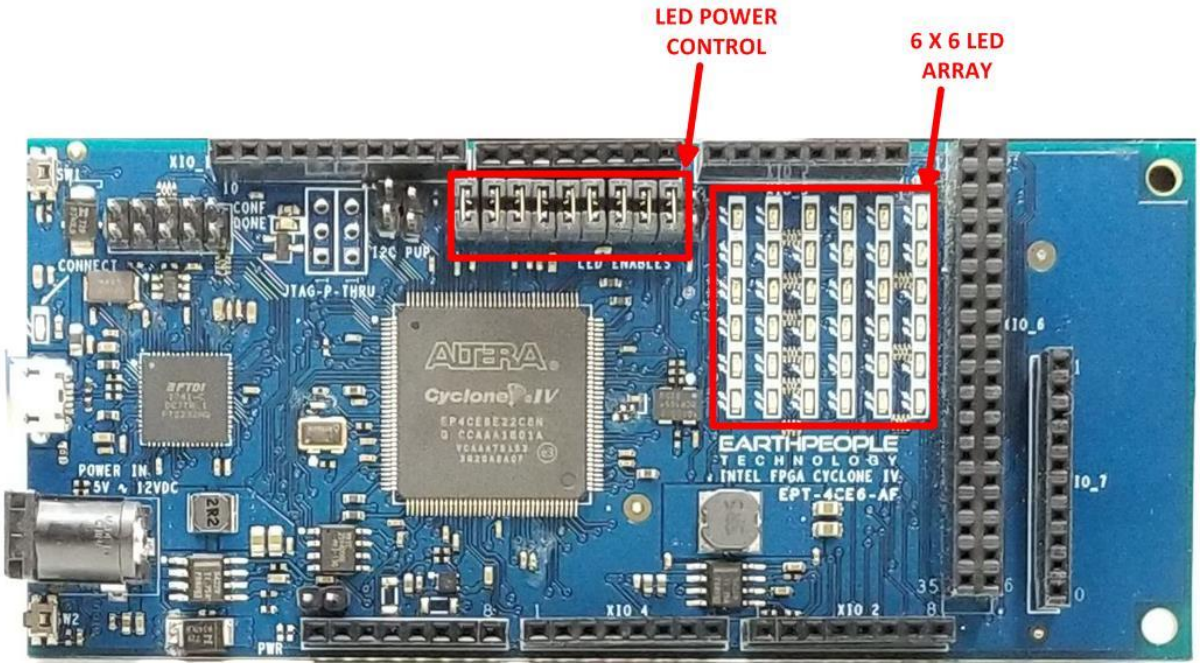
5 LEDs

There are 8 total LEDs on the DueProLogic. Four Green User LEDs and one Green, one Red, one Yellow and one Orange High Impedance dual use LEDs. The four Green User LEDs are driven directly from the Cyclone IV FPGA. The four High Impedance dual use LEDs have Op Amp drivers to allow the pins to be used as user I/Os. These pins are available on the H9 connector.

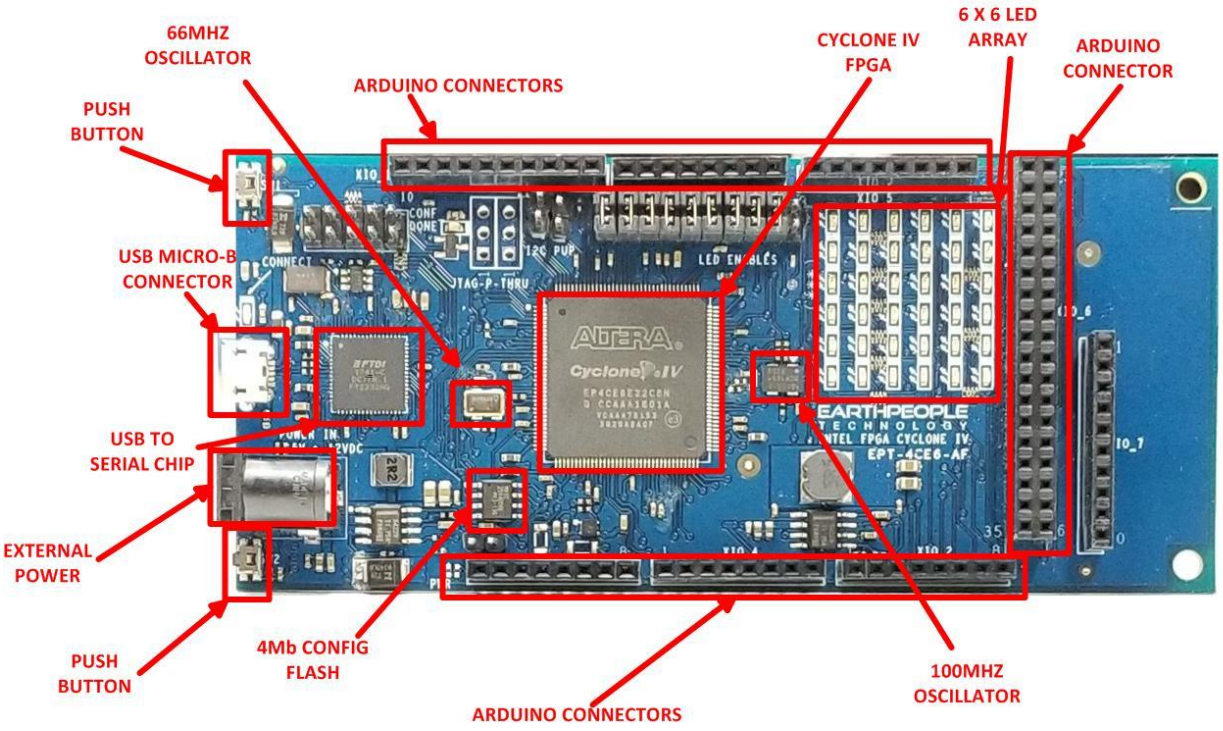
Component	**Net Name**	**Pin on FPGA**	**Signal in EPT Project Pinout**
LED0	UB22	TBD	XIO_6 [0]
LED1	UB23	TBD	XIO_6 [1]
LED2	UB24	TBD	XIO_6 [2]
LED3	UB25	TBD	XIO_6 [3]
LED4	UB26	TBD	XIO_6[4]
LED5	UB27	TBD	XIO_6[5]

LED6	UB28	TBD	XIO_6[6]
LED7	UB29	TBD	XIO_6[7]
LED8	UB30	TBD	XIO_6 [8]
LED9	UB31	TBD	XIO_6 [9]
LED10	UB32	TBD	XIO_6 [10]
LED11	UB33	TBD	XIO_6 [11]
LED12	UB34	TBD	XIO_6[12]
LED13	UB35	TBD	XIO_6[13]
LED14	UB36	TBD	XIO_6[14]
LED15	UB37	TBD	XIO_6[15]
LED16	UB38	TBD	XIO_6 [16]
LED17	UB39	TBD	XIO_6 [17]
LED18	UB40	TBD	XIO_6 [18]
LED19	UB41	TBD	XIO_6 [19]
LED20	UB42	TBD	XIO_6[20]
LED21	UB43	TBD	XIO_6[21]
LED22	UB44	TBD	XIO_6[22]
LED23	UB45	TBD	XIO_6[23]
LED24	UB46	TBD	XIO_6 [24]
LED25	UB47	TBD	XIO_6 [25]
LED26	UB48	TBD	XIO_6 [26]
LED27	UB49	TBD	XIO_6 [27]
LED28	UB50	TBD	XIO_6[28]

LED29	UB51	TBD	XIO_6[29]
LED30	UB52	TBD	XIO_6[30]
LED31	UB53	TBD	XIO_6[31]
LED32	UB68	TBD	XIO_7[0]
LED33	UB69	TBD	XIO_7[1]
LED34	UB70	TBD	XIO_7[2]
LED35	UB71	TBD	XIO_7[3]



6 Inputs/Outputs

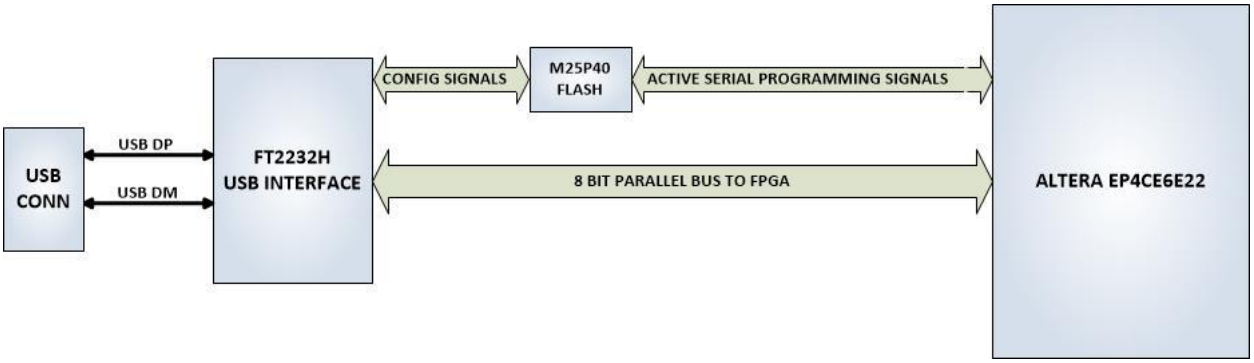


All I/O's are +3.3V only. Do not apply any voltage greater than +3.3V to the FPGA I/O's.

7 FPGA Configuration

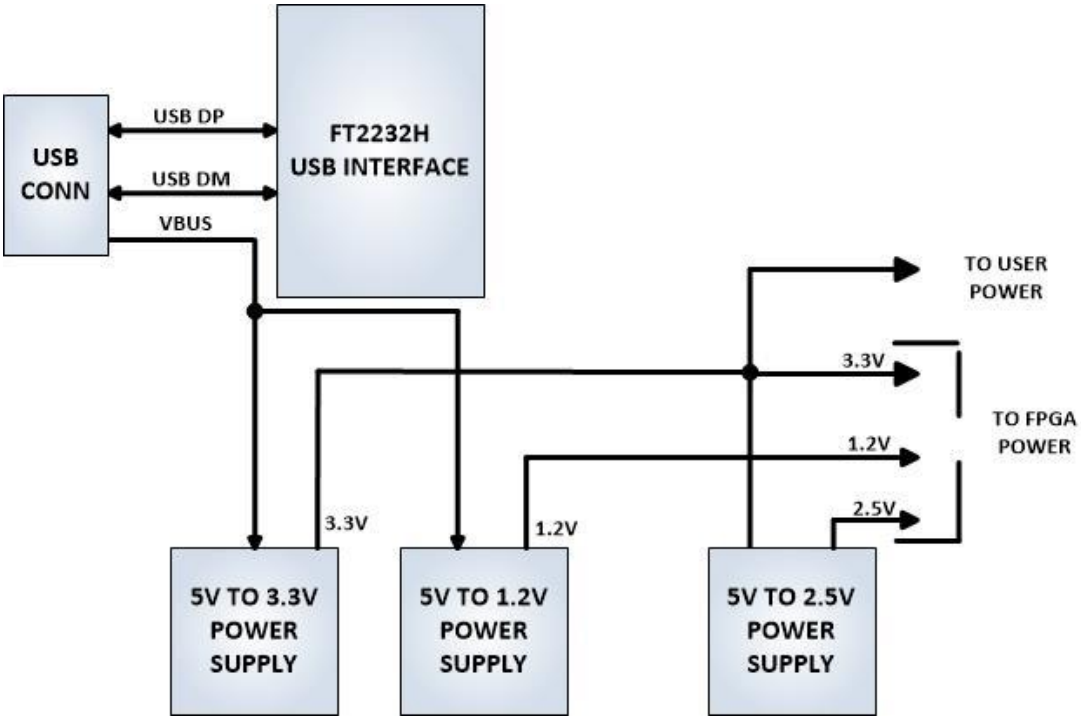
The EPT Blaster Driver will allow the Quartus II Software to program the Configuration Flash chip on the DueProLogic. The software will only access the M25P40 Flash chip. This chip is accessed from the FT2232H USB chip. Quartus will store the compiled and synthesized user code. After programming is complete, the FPGA automatically resets and reads the code from the Flash chip and programs itself

using the Active Serial method.



8 DueProLogic Power

The DueProLogic can be powered from the USB bus of a Host/PC or the optional barrel connector. The USB supplies a maximum of +5V @ 500mA's. The components of the DueProLogic must share this power with the user code that will run inside the FPGA along with any external power use.



1.1.1 Core Board Power Budget

Device	**Part Number**	**+1.2V Power**	**+2.5V Power**	**+3.3V Power**
FPGA	EP4CE6E22	??? Defined by user code. EPT-Transfer-Demo code: 50mA	10mA	??? Defined by user code. . EPT-Transfer-Demo code: 50mA
Flash	M25P40			15mA (During the Write Status, Sector Erase, and Bulk Erase cycles)
USB Chip	FT2232H			60 mA (no sink current supplied to I/O's)
USB EEPROM	93LC56			2 mA (write current) 1 mA (read current)
66MHz Oscillator	FXO-HC536R-66			47 mA
100MHz Oscillator	FXO-HC536R-100			47 mA
Op-Amp driver	MCP6L04			0.5 mA (all four amps active)

User LEDs				20 mA
Green LED				5 mA
Red LED				5mA
Orange LED	ADXL345			5 mA
Yellow LED	TMP100			5 mA
Total		**50mA**	**10mA**	**261mA**

*Theoritical Values only. This data needs to be validated

1.1.2 Core Board VUSB Power Budget

Device	**Part Number**	**VUSB**		
+1.2V Power Supply	ISL9205IRZ	70mA		
+2.5V Power Supply	NCP360MU	12mA		
+3.3V Power Supply	LTC2952	275mA		
Total		**357mA**		

* Theoritical Values only. This data needs to be validated