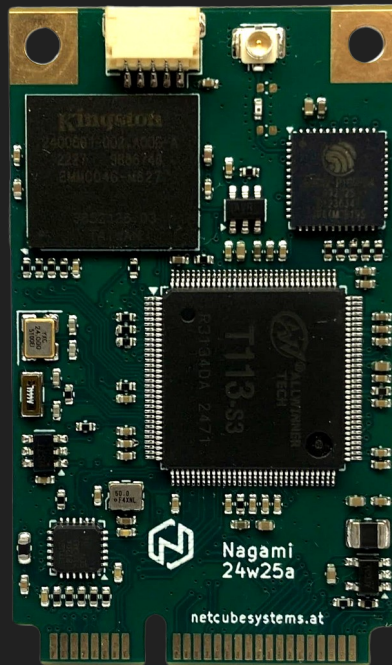




Nagami



The Nagami is a compact and powerful embedded module built around the Allwinner T113-s3 SoC. With dual ARM Cortex-A7 cores, integrated HiFi4 DSP, built-in storage, and rich peripheral options, the Nagami delivers high performance and flexibility in a familiar miniPCIe full-size form factor. It's a perfect fit for demanding industrial, IoT, and embedded applications.

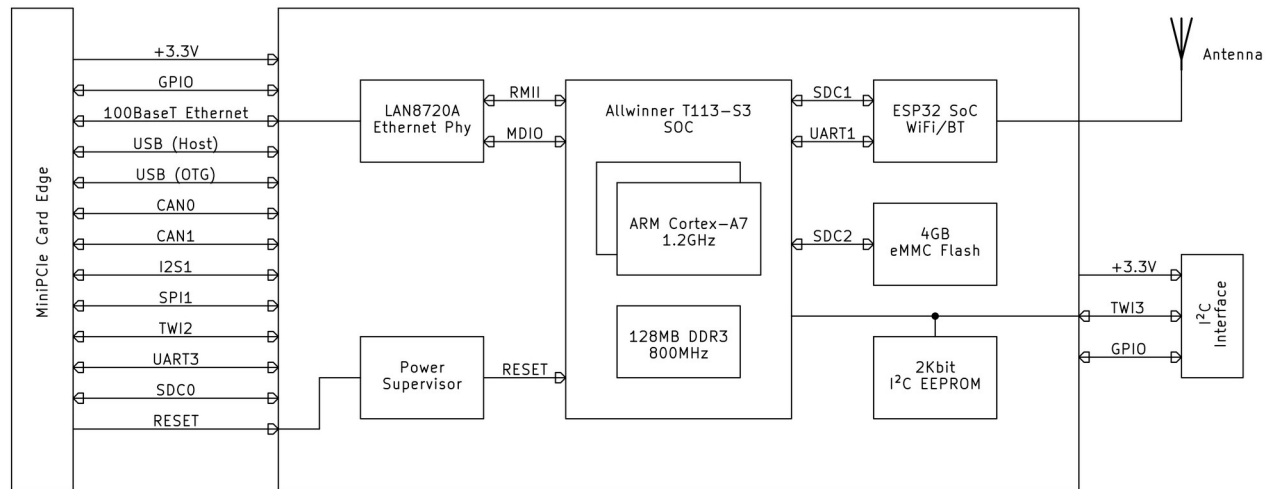
Quick specs

- Dual ARM Cortex-A7 @ 1.2GHz
- 128MB DDR3 Memory, 4GB eMMC
- On-Board 10/100 Mbit Ethernet Phy
- ESP32 with U.FL connector for WiFi/BT
- Buildroot and Alpine Linux images and source
- Standard MiniPCIe connector with custom pinout
- CODESYS SoftPLC capable
- Multiple available interfaces:
 - 1x USB 2.0 OTG, 1x USB 2.0 Host
 - 1x SPI interface with HOLD/WP pins
 - Up to 5 UARTs (2 with RTS/CTS)
 - Up to 4 I2C interfaces
 - Up to 2 CAN 2.0B interfaces
 - Up to 2 I2S/PCM and 1 SPDIF I/O interfaces

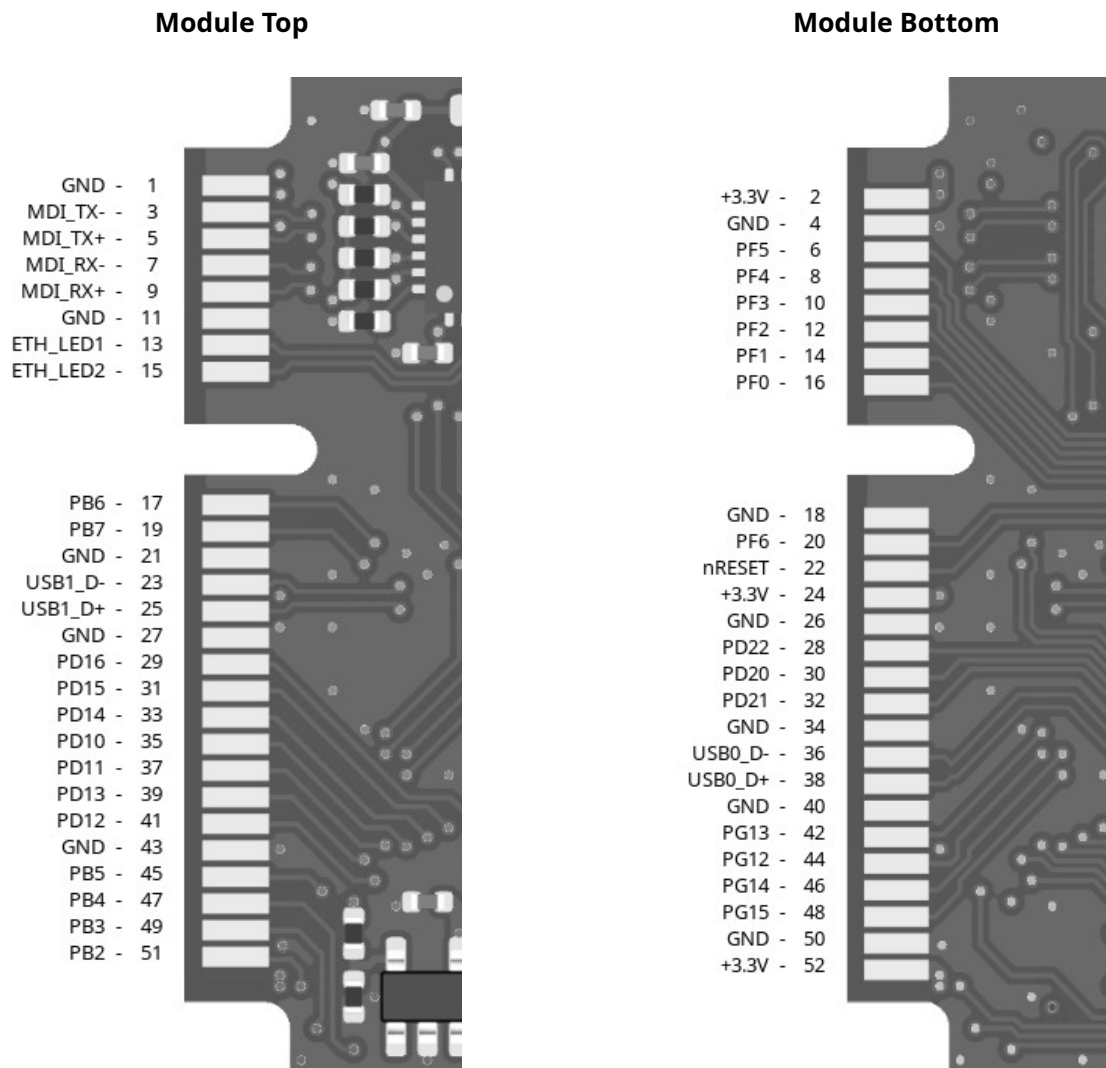
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1. Block diagram



2. Module pinout and pin description



2.1. Module Pad Types

Symbol	Description
PI	Power input
I/O	Digital bidirectional signal
GND	Ground
AO	Analog output
AI	Analog input
PO	Power output
O	Digital output signal
I	Digital input signal

2.2. Power, Ground and Reset

Pin	Pin name	Type	Description
2, 24, 52	+3.3V	PI	+3.3V power supply
22	nRESET	I	Hardware reset
1, 4, 11, 18, 21, 26, 27, 34, 40, 43, 50	GND	GND	Ground connection

2.3. Ethernet

Pin	Pin name	Type	Description
3	MDI_TX-	AO	Ethernet transmit negative signal
5	MDI_TX+	AO	Ethernet transmit positive signal
7	MDI_RX-	AI	Ethernet receive negative signal
9	MDI_RX+	AI	Ethernet receive positive signal
13	ETH_LED1	O	Ethernet link/activity LED 1 (Speed)
15	ETH_LED2	O	Ethernet link/activity LED 2 (Link/Act)

2.4. USB

Pin	Pin name	Type	Description
36	USB0_D-	AI/AO	USB OTG data negative signal
38	USB0_D+	AI/AO	USB OTG data positive signal
23	USB1_D-	AI/AO	USB Host data negative signal
25	USB1_D+	AI/AO	USB Host data positive signal

2.5. CAN

Pin	Pin name	Type	Description
49	CAN0_RX	I	CAN0 receive signal
51	CAN0_TX	O	CAN0 transmit signal
45	CAN1_RX	I	CAN1 receive signal
47	CAN1_TX	O	CAN1 transmit signal

2.6. I2C

Pin	Pin name	Type	Description
30	TWI2_SCK	O	I2C clock signal
32	TWI2_SDA	IO	I2C data signal

2.7. I2S

Pin	Pin name	Type	Description
42	I2S1_BCLK	O	I2S bit clock signal
44	I2S1_LRCK	O	I2S left/right clock signal
46	I2S1_DIN0	I	I2S data input channel 0
48	I2S1_DOUT0	O	I2S data output channel 0

2.8. UART

Pin	Pin name	Type	Description
17	UART3_TX	O	UART transmit signal
19	UART3_RX	I	UART receive signal

2.9. SD

Pin	Pin name	Type	Description
12	SDC0_CLK	O	SD clock signal
10	SDC0_CMD	IO	SD command signal
14	SDC0_D0	IO	SD data line 0
16	SDC0_D1	IO	SD data line 1
6	SDC0_D2	IO	SD data line 2
8	SDC0_D3	IO	SD data line 3

2.10. SPI

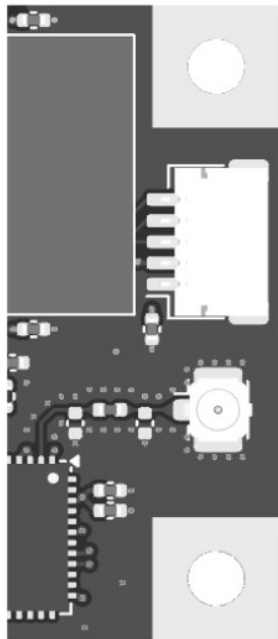
Pin	Pin name	Type	Description
37	SPI1_CLK	O	SPI clock signal
41	SPI1_MOSI	O	SPI master out, slave in signal
39	SPI1_MISO	I	SPI master in, slave out signal
35	SPI1_CS	O	SPI chip select signal
31	SPI1_WP	O	SPI write protect signal (optional)
33	SPI1_HOLD	O	SPI hold signal (optional)

2.11. GPIO

Pin	Pin name	Type	Description
20	PF6	IO	General-purpose input/output pin PF6
28	PD22	IO	General-purpose input/output pin PD22
29	PD16	IO	General-purpose input/output pin PD16

2.12. External I2C

There is a secondary I2C bus and interrupt line exposed on a 5-Pin JST-SH next to the WiFi/BT Antenna connector.



5 - PE10
4 - PG10
3 - PG11
2 - +3.3V
1 - GND

1 - WiFi/BT

Pin	Pin name	Type	Description
1	GND	GND	Ground connection
2	+3.3V	PO	+3.3V power supply
3	TWI3_SDA	AI	I2C data signal shared with EEPROM
4	TWI3_SCK	AI	I2C clock signal shared with EEPROM
5	PE10	O	Dedicated GPIO for I2C Interrupt on PE10

3. Alternative pin functions

	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
51	PB2 LCD0-D0	I2S2-DOUT2	TWI0-SDA	I2S2-DIN2	LCD0-D18	UART4-TX	CAN0_TX0	PB-EINT2
49	PB3 LCD0-D1	I2S2-DOUT1	TWI0-SCK	I2S2-DIN0	LCD0-D19	UART4-RX	CAN0_RX0	PB-EINT3
47	PB4 LCD0-D8	I2S2-DOUT0	TWI1-SCK	I2S2-DIN1	LCD0-D20	UART5-TX	CAN1_TX0	PB-EINT4
45	PB5 LCD0-D9	I2S2-BCLK	TWI1-SDA	PWM0	LCD0-D21	UART5-RX	CAN1_RX0	PB-EINT5
17	PB6 LCD0-D16	I2S2-LRCK	TWI3-SCK	PWM1	LCD0-D22	UART3-TX	CPUBIST0	PB-EINT6
19	PB7 LCD0-D17	I2S2-MCLK	TWI3-SDA	IR-RX	LCD0-D23	UART3-RX	CPUBIST1	PB-EINT7
35	PD10 LCD0-D14	LVDS1-V0P	SPI1-CS	UART3-TX				PD-EINT10
37	PD11 LCD0-D15	LVDS1-V0N	SPI1-CLK	UART3-RX				PD-EINT11
41	PD12 LCD0-D18	LVDS1-V1P	SPI1-MOSI	TWI0-SDA				PD-EINT12
39	PD13 LCD0-D19	LVDS1-V1N	SPI1-MISO	UART3-RTS				PD-EINT13
33	PD14 LCD0-D20	LVDS1-V2P	SPI1-HOLD	UART3-CTS				PD-EINT14
31	PD15 LCD0-D21	LVDS1-V2N	SPI1-WP	IR-RX				PD-EINT15
29	PD16 LCD0-D22	LVDS1-CKP	DMIC-DATA3	PWM0				PD-EINT16
30	PD20 LCD0-HSYNC	TWI2-SCK	DMIC-CLK	PWM4				PD-EINT20
32	PD21 LCD0-VSYNC	TWI2-SDA	UART1-TX	PWM5				PD-EINT21
28	PD22 OWA-OUT	IR-RX	UART1-RX	PWM7				PD-EINT22
16	PF0 SDC0-D1	JTAG-MS		I2S2-DOUT1	I2S2-DIN0			PF-EINT0
14	PF1 SDC0-D0	JTAG-DI		I2S2-DOUT0	I2S2-DIN1			PF-EINT1
12	PF2 SDC0-CLK	UART0-TX	TWI0-SCK	LEDC-DO	OWA-IN			PF-EINT2
10	PF3 SDC0-CMD	JTAG-DO		I2S2-BCLK				PF-EINT3
8	PF4 SDC0-D3	UART0-RX	TWI0-SDA	PWM6	IR-TX			PF-EINT4
6	PF5 SDC0-D2	JTAG-CK		I2S2-LRCK				PF-EINT5
20	PF6	OWA-OUT	IR-RX	I2S2-MCLK	PWM5			PF-EINT6
44	PG12 I2S1-LRCK	TWI0-SCK	II-TXCTRL/RMII-7	CLK-FANOUT2	PWM0	UART1-TX		PG-EINT12
42	PG13 I2S1-BCLK	TWI0-SDA	III-CLKIN/RMII-R	PWM2	LEDC-DO	UART1-RX		PG-EINT13
46	PG14 I2S1-DIN0	TWI2-SCK	MDC	I2S1_DOUT1	SPI0-WP	UART1-RTS		PG-EINT14
48	PG15 I2S1-DOUT0	TWI2-SDA	MDIO	I2S1_DIN1	SPI0-HOLD	UART1-CTS		PG-EINT15

4. Electrical characteristics

4.1. Recommended operating conditions

Parameter	Unit	Minimum	Typical	Maximum
Ambient Operating Temperature (with Heat sink)	°C	-25	-	85
Ambient Operating Temperature (without Heat sink)	°C	-25	-	75
Supply voltage (+3.3V)	V	2.97	3.3	3.63

4.2. Power consumption parameters

Parameter	Unit	Minimum	Typical	Maximum
Main supply (+3.3V)	mA			1200

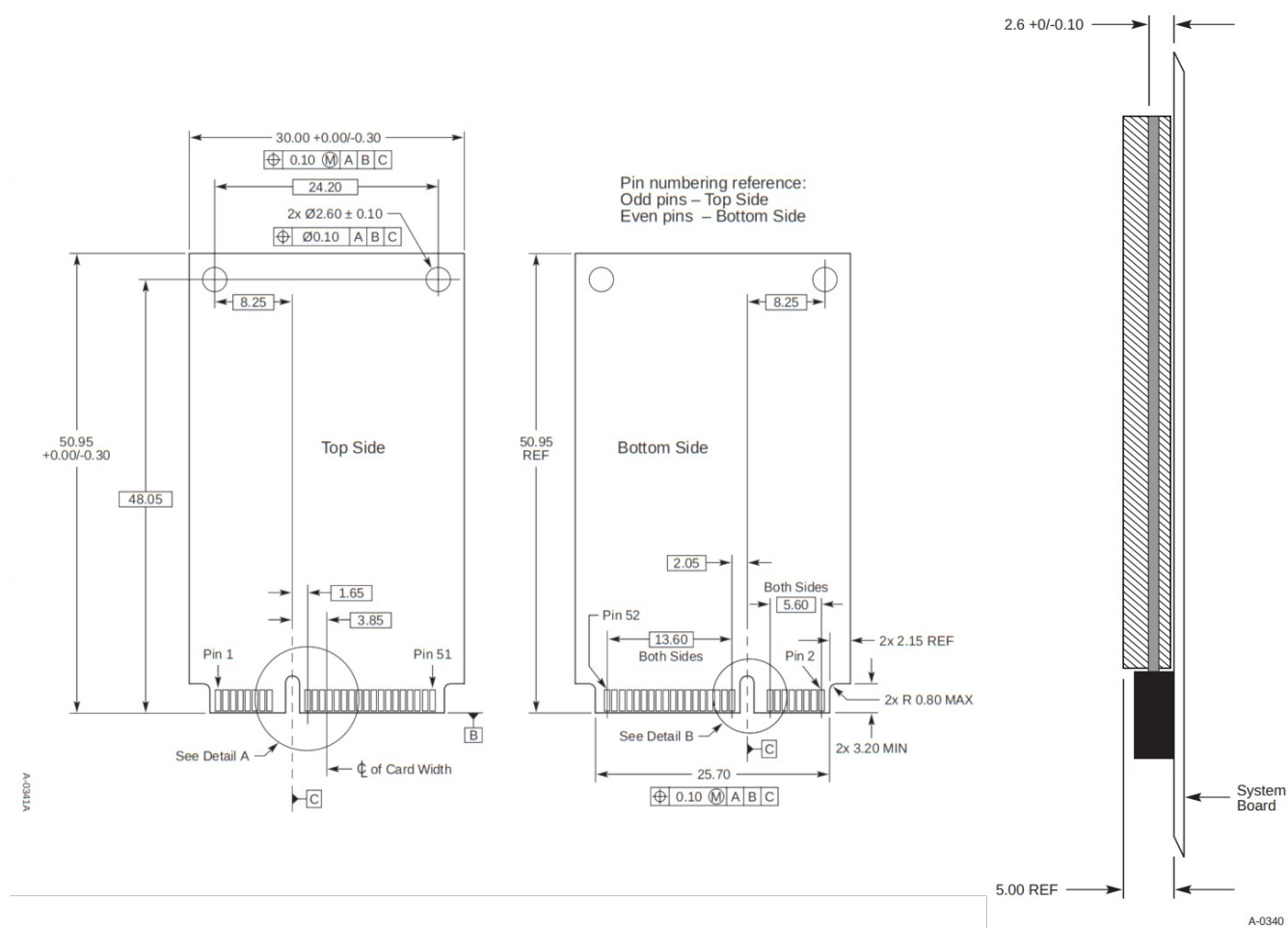
4.3. DC electrical characteristics

Parameter	Unit	Minimum	Typical	Maximum
High-Level Input Voltage	V	0.7 * (+3.3V)	-	(+3.3V) + 0.3
Low-Level-Input Voltage	V	-0.3	-	0.3 * (+3.3V)
Input Pull-up Resistance (PF3, PF6)	kΩ	12	15	18
Input Pull-up Resistance (Other GPIOs)	kΩ	80	100	120
Input Pull-down Resistance (PF3, PF6)	kΩ	12	15	18

Parameter	Unit	Minimum	Typical	Maximum
Input Pull-down Resistance (Other GPIOs)	k Ω	80	100	120
Output drive current	MA	-	-	6

5. Mechanical characteristics

5.1. Module dimension



6. Useful external documents

Document	Link
MiniPCIe Mechanical Spec	https://heap.ovh/files/mPCIe-electromechanical.pdf
ESP32 Datasheet	https://www.espressif.com/sites/default/files/documentation/esp32-pico_series_datasheet_en.pdf
Linux SUNXI Wiki on T113-s3	https://linux-sunxi.org/T113-s3
Allwinner T113-s3 Datasheet	https://linux-sunxi.org/images/7/73/T113-s3_datasheet_v1.6.pdf
Allwinner T113-s3 User Manual	https://bbs.aw-ol.com/assets/uploads/files/1648883311855-t113-s3_user_manual_v1.1.pdf
Nagami ReadTheDocs	https://nagami.rtfid.io/

7. Document history

Version	Date	Description
V1.2	16.12.2025	Remove QWIIC-Compatible references and add pinout for I2C connector
V1.1	20.07.2025	Fix minor typos
V1.0	12.07.2025	Initial release