Tynemouth Software

TYNEMOUTH MINSTREL INPUT MONITOR

OVERVIEW

This is way of monitoring key presses and tape load data via LEDs and optionally a piezo sounder for Minstrel 2, Minstrel 3 or ZX81.

It is designed for the Minstrel Expansion Bus, but could be built with an edge connector for direct connection to one of those machines.

PARTS LIST

CAPACITORS – CERAMIC RATED 6.3V OR HIGHER

3 x 100nF axial *(usually marked 100n or 104)*

RESISTORS – ALL ¼W 5% OR BETTER (4 BAND RESISTOR COLOUR CODES SHOWN)

3 x 470Ω 

SEMICONDUCTORS – NEW TEXAS INSTRUMENTS PARTS RECOMMENDED

1 x 74HC11
1 x 74HC32
1 x 74HC74
1 x Red 5mm LED
1 x Green 5mm LED

CONNECTORS / SOUNDER

2x23 way 0.1” straight pin header or 2x23 way 0.1” card edge connector
2x3 way 0.1” straight pin header with jumpers
1 x Piezo AC transducer *(not a buzzer or any sounder that has internal circuitry)*
3 x 14 pin IC sockets *(Optional, turned pin recommended if fitted)*

ASSEMBLY

Assembly should be straight forward, starting with the axial capacitors, resistors, then ICs (or IC sockets if used) and finally the jumper block, LEDs and piezo.

The pin header or edge connector is soldered to the pads at the bottom of the board. In both cases, the third pin from the left, front and back, should be removed for polarisation.

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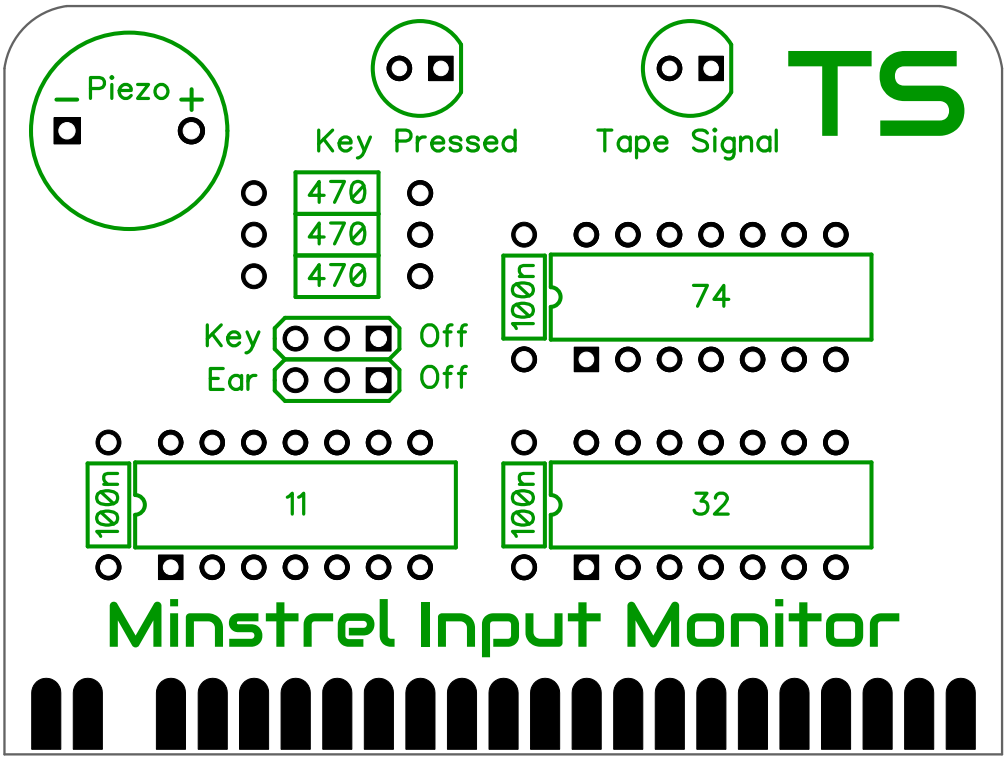
COMPONENT PLACEMENT

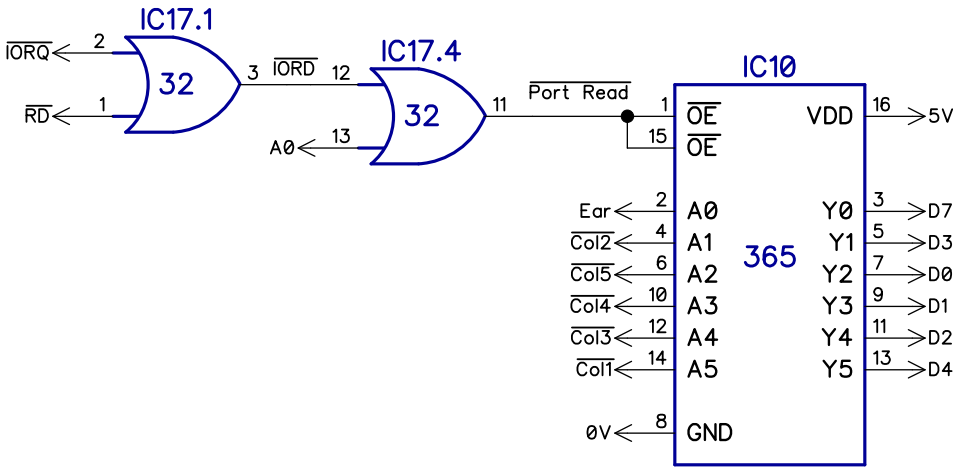


THEORY OF OPERATION

INPUT PORT

The Minstrel and ZX81 have a single input port. This is used to read the keyboard and tape data from the earphone socket.

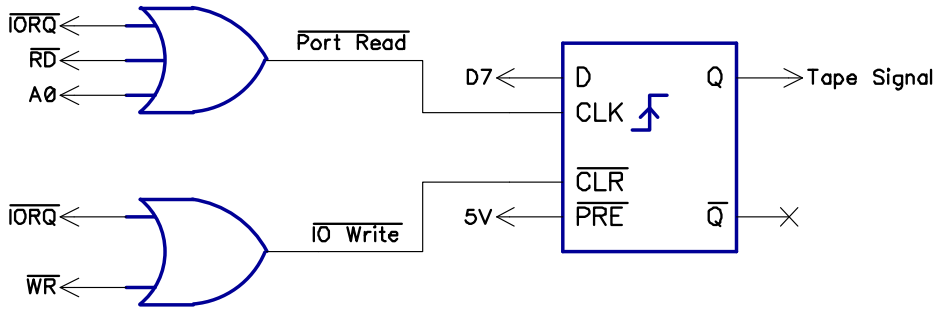
The Minstrel 2 / ZX80 input port is shown here as that is the simplest version.



When the Z80 makes an IO read request and the address is even (A0 is low) the 74LS365 will place the inputs on the databus in time for the Z80 to read the bus on the rising edge of the IO request.

TAPE SIGNAL

The Minstrel Input Monitor duplicates that decoding and a 74HC74 flip flop is triggered on the rising edge of the port read signal to read the data from the bus.



At this point, it samples D7, the data from the tape as the Z80 will see it, digital data, rather than the analogue tape input signal.

During loading, this port is repeatedly read for each bit, so the Tape Signal output will mirror this data.

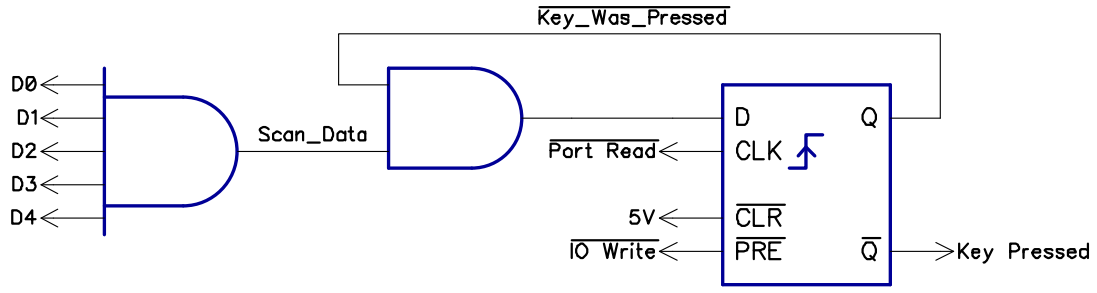
If loading fails, it will stop reading the port, so the LED will stop flashing, a useful indication.

At the end of loading, the screen draw restarts with an IO write. This clears the flip flop.

KEYBOARD SCAN

The keyboard can be checked in a similar way. It is read once at the top of each screen draw cycle. For that first scan, the keyboard rows are setup so that if any keys are pressed, one of the data lines will be low.

If that is detected, then each of the 8 rows are scanned separately.



The Minstrel Input Monitor uses the second half of the flip flop to latch the scanned data on the port read.

Any rows that have a key pressed will set the Key Pressed signal high, but any rows that have no keys pressed will set it low again.

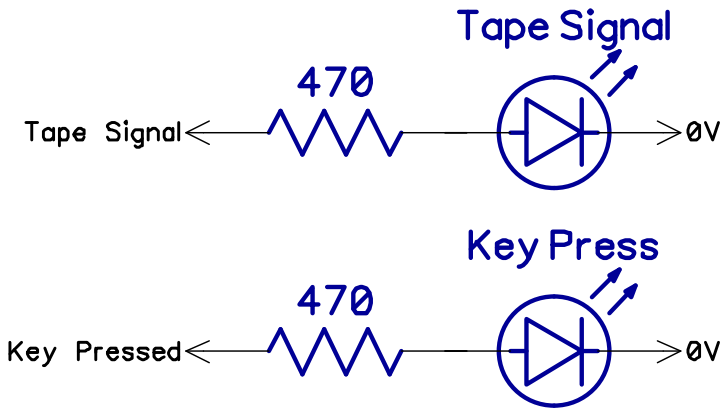
The second AND gate here combines the keyboard scan data with the previous state, so if a key has been pressed, Key Pressed will remain high even if a row is scanned with no keys pressed.

If a key was pressed, the Key Pressed signal will remain high until the display drawing beings with an IO write, which will clear the flip flop so Key Pressed will go low.

This sequence happens at the start of every frame, so this will create a 50Hz tone on the piezo if any keys are pressed.

LEDS

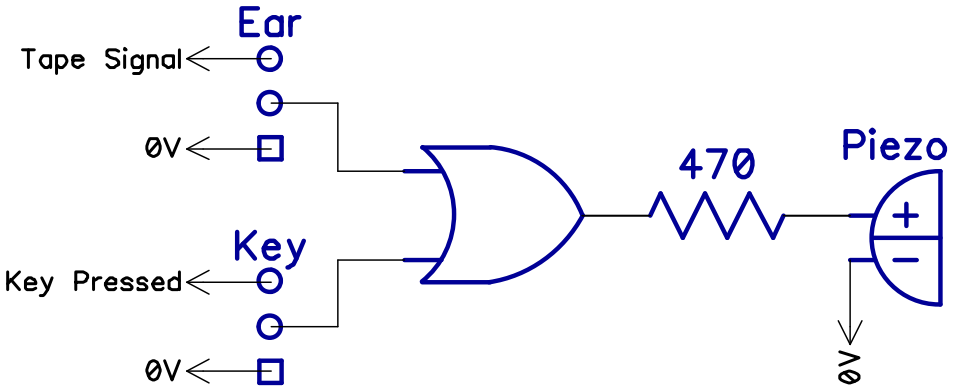
The signals generated will be high when active, one if there is a key pressed, one when the tape data is high.



Two LEDs are used to show the state of those signals. I have used green for a key press and red for tape data.

PIEZO SOUNDER

Audio indication of the two signals can be provided by a piezo sounder.



The OR gate mixes the signals to drive the piezo sounder.

Jumpers are provided to disable either signal before the mixer, in case the sound becomes annoying.

IMPLEMENTATION

The schematics above use ideal arrangement of gates, but it is not possible to easily get a 5 input AND gates, or the other assortment of 2 and 3 input AND and OR gates on just a few chips.

The actual implementation uses a quad 2 input OR gate and a triple 3 input AND gate, to implement the same logic, as shown in the complete schematic.

FULL SCHEMATIC

The schematics snippets above use ideal arrangement of gates, but it is not possible to easily get a 5 input AND gates, or the other assortment of 2 and 3 input AND and OR gates on just a few chips.

The actual implementation uses a quad 2 input OR gate and a triple 3 input AND gate, to implement the same logic.