OneChipBook Series - 12

Technical Reference

Document Revision 1.0

Overview

The OneChipBook-12 is an FPGA development platform centered around the Cyclone EP1C12Q core. It integrates a VGA monitor, PS/2 mechanical keyboard, battery, and I/O ports. All peripheral devices are connected to the FPGA's general-purpose I/O pins, allowing users to control the entire system by developing for a single chip without complex interface design.

OneChipBook-12 has two order numbers. They share identical keyboard scan codes, with the only difference being the keyboard silkscreen markings.

- OneChipBook -12 (12k Les) -A (Keyboard layout A)
  -B (Keyboard layout B)

Features

- FPGA: Cyclone EP1C12Q240
  - 12,060 Les
  - 239,616 bits RAM
- 32MB SDRAM
- 1024x768 VGA monitor
- VGA/S-Video/CVBS Output interface
- Mechanical keyboard (PS/2)/ Backlight
- Stereo speakers
- Type-C charging port
- Lithium battery
- Expansion Bus Support

Keyboard layout

- Keyboard layout A

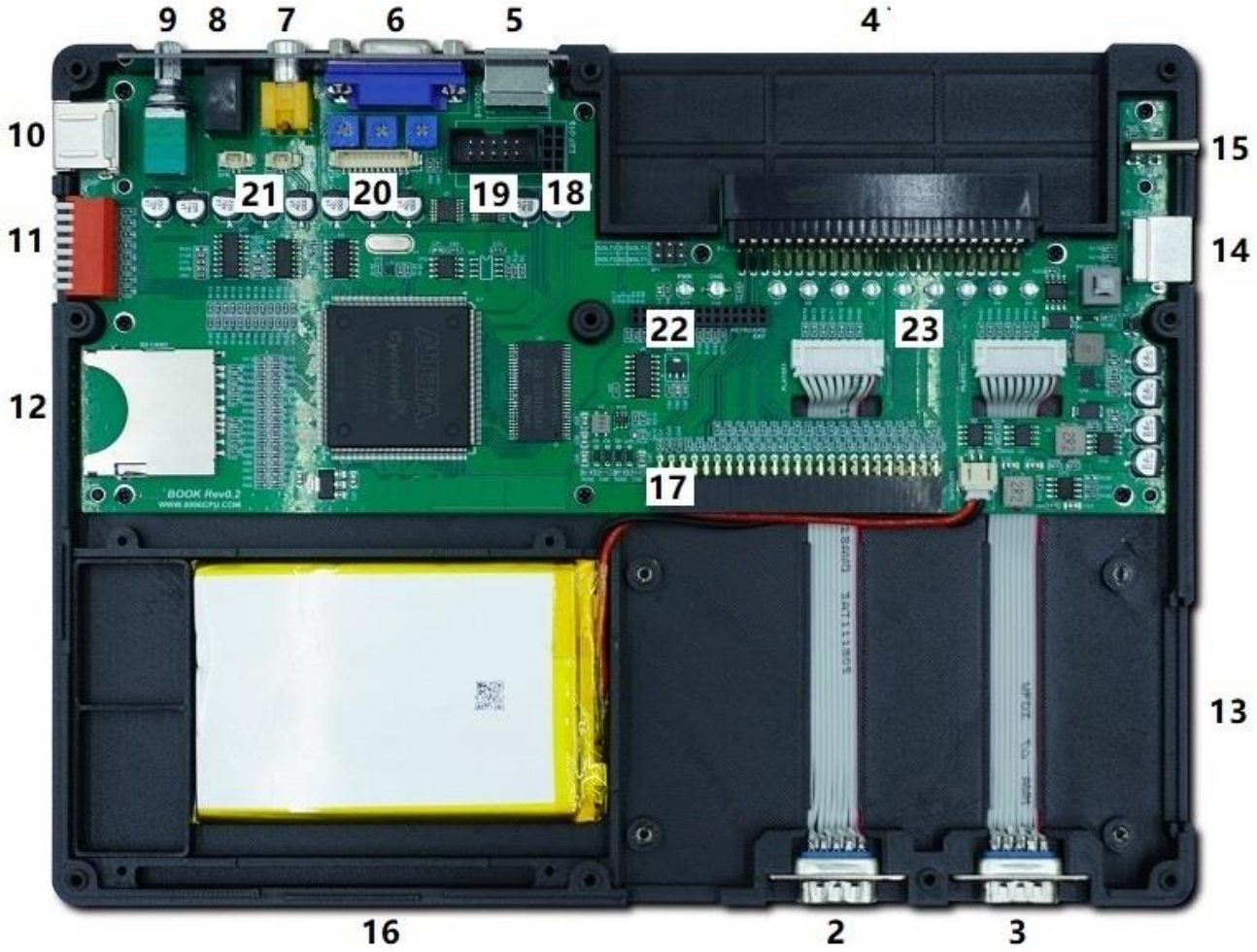
- Keyboard layout B

External Interfaces

1. Firmware download port. (Active Serial Programming)
2. 1# DB9 Port
3. 2# DB9 Port
4. External expansion slot
5. S-Video interface
6. VGA interface
7. CVBS interface
8. Audio output jack
9. Volume control knob
10. USB port
11. Setting switch
12. SD card slot
13. Input/output window with built-in expansion card
14. PS/2 Keyboard port
15. Type-C charging port (5V-2A)

Motherboard

The OneChipBook-12's motherboard employs a four-layer PCB manufacturing process. Inside the device, there is an expansion interface that utilizes the same I/O as the external expansion slot, allowing users to design custom expansion modules and install them into the internally reserved space.

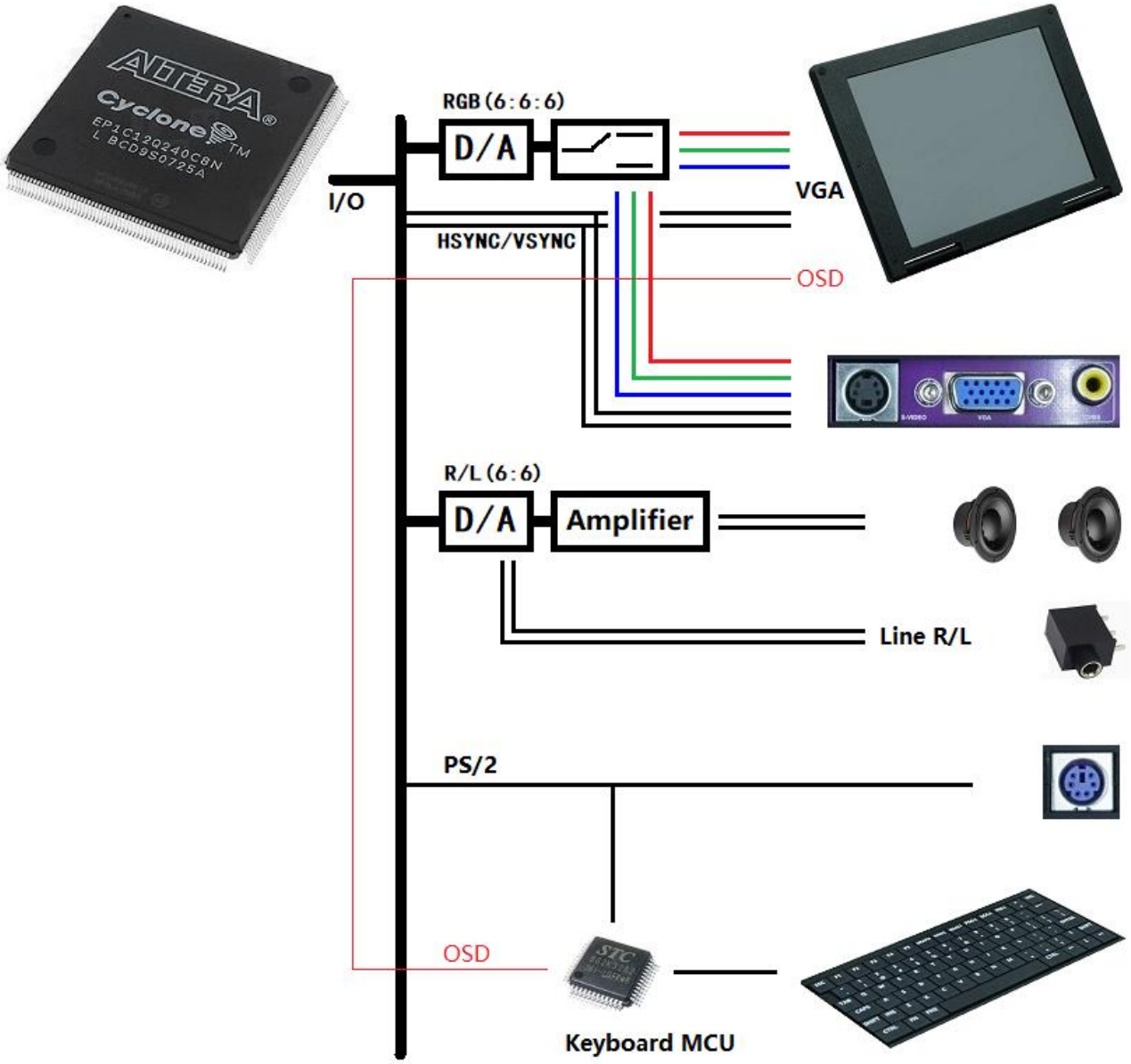


16. Battery compartment
17. Built-in expansion crad slot
18. Built-in module Interface
19. Firmware download port. (Active Serial Programming)
20. VGA monitor Interface
21. Speaker Interface
22. Built-in keyboard Interface
23. Status LED*9

Functional Description

1. Video / Audio / Keyboard

- The OneChipBook-12's LCD screen can be considered a built-in VGA monitor. It receives VGA signals, eliminating the need for users to manage LCD control. Whether the VGA signal is routed to the internal LCD monitor or the external VGA port is determined by a video toggle switch on the motherboard.
- The audio system consists of a D/A converter circuit, an amplifier, speakers, and output ports.
- The built-in keyboard is controlled by an MCU and outputs PS/2 protocol keyboard scan codes. It is connected in parallel with the external PS/2 port. To use an external PS/2 keyboard, the built-in keyboard can be disabled first. The integrated system of built-in keyboard → MCU → LCD operates independently of the FPGA, forming an On-Screen Display (OSD) system that provides users with fundamental keyboard and LCD configuration settings.



- Pin assignment:

VGA	
	FPGA Pin
HSYNC	75
VSYNC	74

RED	
VR5	104
VR4	101
VR3	100
VR2	99
VR1	98
VR0	95

GREEN	
VG5	94
VG4	93
VG3	88
VG2	87
VG1	86
VG0	85

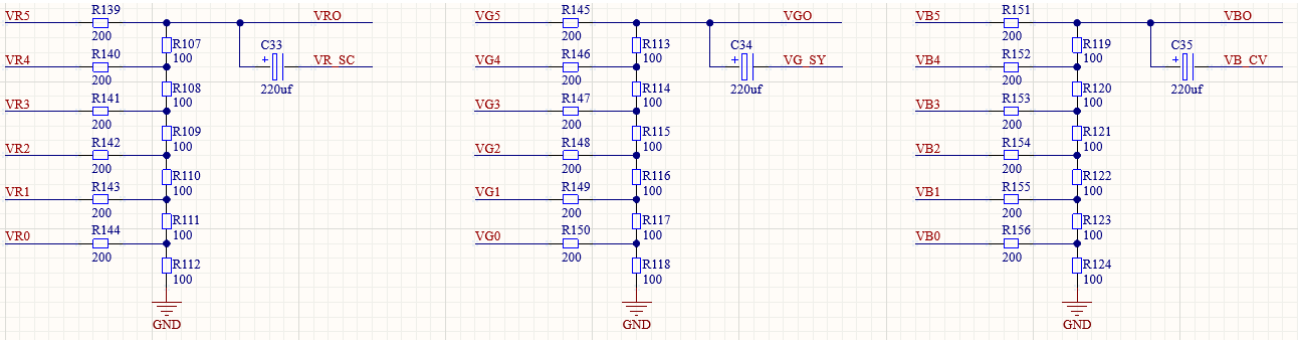
BLUE	
VB5	84
VB4	83
VB3	82
VB2	79
VB1	78
VB0	77

PS2/Keyboard	
CLK	68
DATA	67

Audio-R	FPGA Pin
SR5	120
SR4	119
SR3	118
SR2	117
SR1	116
SR0	115

Audio-L	FPGA Pin
SL5	114
SL4	113
SL3	108
SL2	107
SL1	106
SL0	105

- Schematic diagram of the D/A converter circuit (VGA, S-Video, and Composite share these channels via multiplexing)



- The built-in keyboard allows redefinition of scan codes for the F7, INS, ALT, and RCTRL keys to accommodate diverse user needs (refer to the OSD section for configuration).

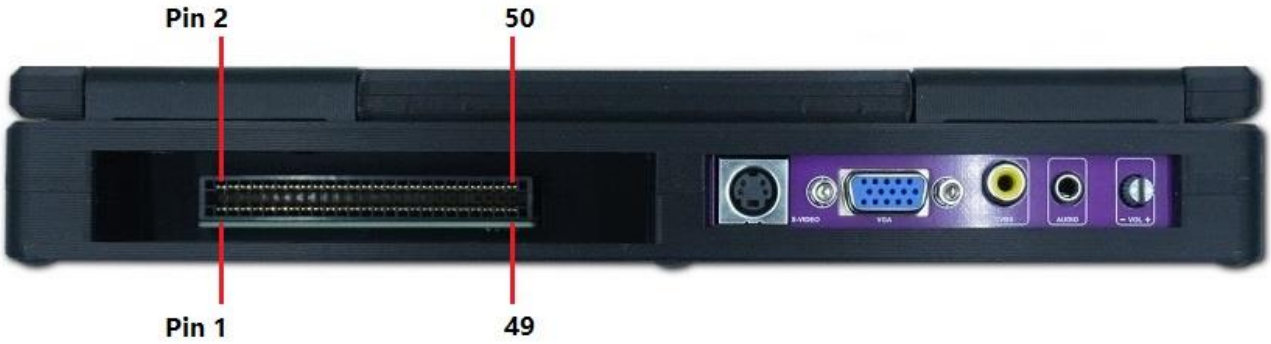
KEY	MAKE CODE	BREAK CODE
A	1C	F0 1C
B	32	F0 32
C	21	F0 21
D	23	F0 23
E	24	F0 24
F	2B	F0 2B
G	34	F0 34
H	33	F0 33
I	43	F0 43
J	3B	F0 3B
K	42	F0 42
L	4B	F0 4B
M	3A	F0 3A
N	31	F0 31
O	44	F0 44
P	4D	F0 4D
Q	15	F0 15
R	2D	F0 2D
S	1B	F0 1B
T	2C	F0 2C
U	3C	F0 3C
V	2A	F0 2A
W	1D	F0 1D
X	22	F0 22
Y	35	F0 35
Z	1A	F0 1A
1	16	F0 16
2	1E	F0 1E
3	26	F0 26
4	25	F0 25
5	2E	F0 2E
6	36	F0 36
7	3D	F0 3D
8	3E	F0 3E
9	46	F0 46
0	45	F0 45
BACK	66	F0 66
SPACE	29	F0 29
TAB	0D	F0 0D
CAPS	58	F0 58
SHIFT	12	F0 12
ENTER	5A	F0 5A
DEL	E0 71	E0 F0 71
ESC	76	F0 76

KEY		MAKE CODE	BREAK CODE
` ~		0E	F0 0E
- _		4E	F0 4E
= +		55	F0 55
\ |		5D	F0 5D
; :		4C	F0 4C
' "		52	F0 52
, <		41	F0 41
. >		49	F0 49
/ ?		4A	F0 4A
[{		54	F0 54
] }		5B	F0 5B
UP		E0 75	E0 F0 75
LEFT		E0 6B	E0 F0 6B
DOWN		E0 72	E0 F0 72
RIGHT		E0 74	E0 F0 74
PrintScreen		E0 12 E0 7C	E0 F0 7C E0 F0 12
Scroll Lock		7E	F0 7E
LCTRL		14	F0 14
F1		05	F0 05
F2		06	F0 06
F3		04	F0 04
F4		0C	F0 0C
F5		03	F0 03
F6		0B	F0 0B
F7	F7	83	F0 83
	INS	E0 70	E0 F0 70
	HOME	E0 6C	E0 F0 6C
F8		0A	F0 0A
F9		01	F0 01
F10		09	F0 09
F11		78	F0 78
INS	INS	E0 70	F0 E0 70
	F7	83	F0 83
	HOME	E0 6C	E0 F0 6C
	F6	0B	F0 0B
	F8	0A	F0 0A
ALT	ALT	11	F0 11
	END	E0 69	E0 F0 69
	HOME	E0 6C	E0 F0 6C
RCTRL	CTRL	14	F0 14
	F7	83	F0 83
	HOME	E0 6C	E0 F0 6C
	F6	0B	F0 0B
	F8	0A	F0 0A

2. External expansion slot

The OneChipBook-12 features a 50-pin external expansion slot that can be used for circuit design extensions or expansion cartridges. This slot consists of:

- 42 general-purpose I/O pins
- 1 reset signal(active-low)
- Power supply lines



- Pin assignment:

	FPGA Pin			FPGA Pin	
IO	122	1	2	123	IO
IO	124	3	4	125	IO
IO	126	5	6	127	IO
IO	128	7	8	131	IO
IO	132	9	10	133	IO
IO	134	11	12	135	IO
IO	136	13	14	137	IO
RESET	153	15	16	138	IO
IO	139	17	18	140	IO
IO	141	19	20	143	IO
IO	156	21	22	158	IO
IO	159	23	24	160	IO
IO	161	25	26	162	IO
IO	163	27	28	164	IO
IO	165	29	30	166	IO
IO	167	31	32	168	IO
IO	169	33	34	170	IO
IO	173	35	36	174	IO
IO	175	37	38	176	IO
IO	177	39	40	178	IO
GND		41	42	144	IO
GND		43	44	179	IO
+5V		45	46	180	IO
+5V		47	48	+12V	
Audio-L		49	50	-12V	

- **Custom Slot Adapter:**
  Users can provide us with the required pin count, specifications, power, and I/O layout configuration for the slot to customize the adapter. (Total usable I/O remains 43 pins.)
  (Picture: Slot adapter appearance illustration)

- Slot Adapter Usage Demonstration: Adapting to Different Cartridge Standards

3. I/O Assignment Table for USB / DIP Switches / Status LEDs / DB9 Interface

- DIP Switches:
  Switch 1# & 2#: Connected to FPGA and serve as control terminals for the VGA line scan generator.
  Other Switches: Connected solely to the FPGA.

- Pin assignment:

DIP-SW	FPGA Pin
1	53
2	54
3	55
4	56
5	57
6	58
7	59
8	60

LED	FPGA Pin
1	43
2	44
3	45
4	46
5	47
6	48
7	49
8	50
9	240

SD	FPGA Pin
DAT0	62
DAT1	61
DAT2	66
DAT3	65
CLK	63
CMD	64

1#DB9	FPGA Pin
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	GND
9	VCC

USB	FPGA Pin
DP2	239
DN2	238

2#DB9	FPGA Pin
1	8
2	11
3	12
4	13
5	14
6	15
7	16
8	GND
9	VCC

4. SDRAM

OneChipBook-12 is equipped with one SDRAM(32MB).

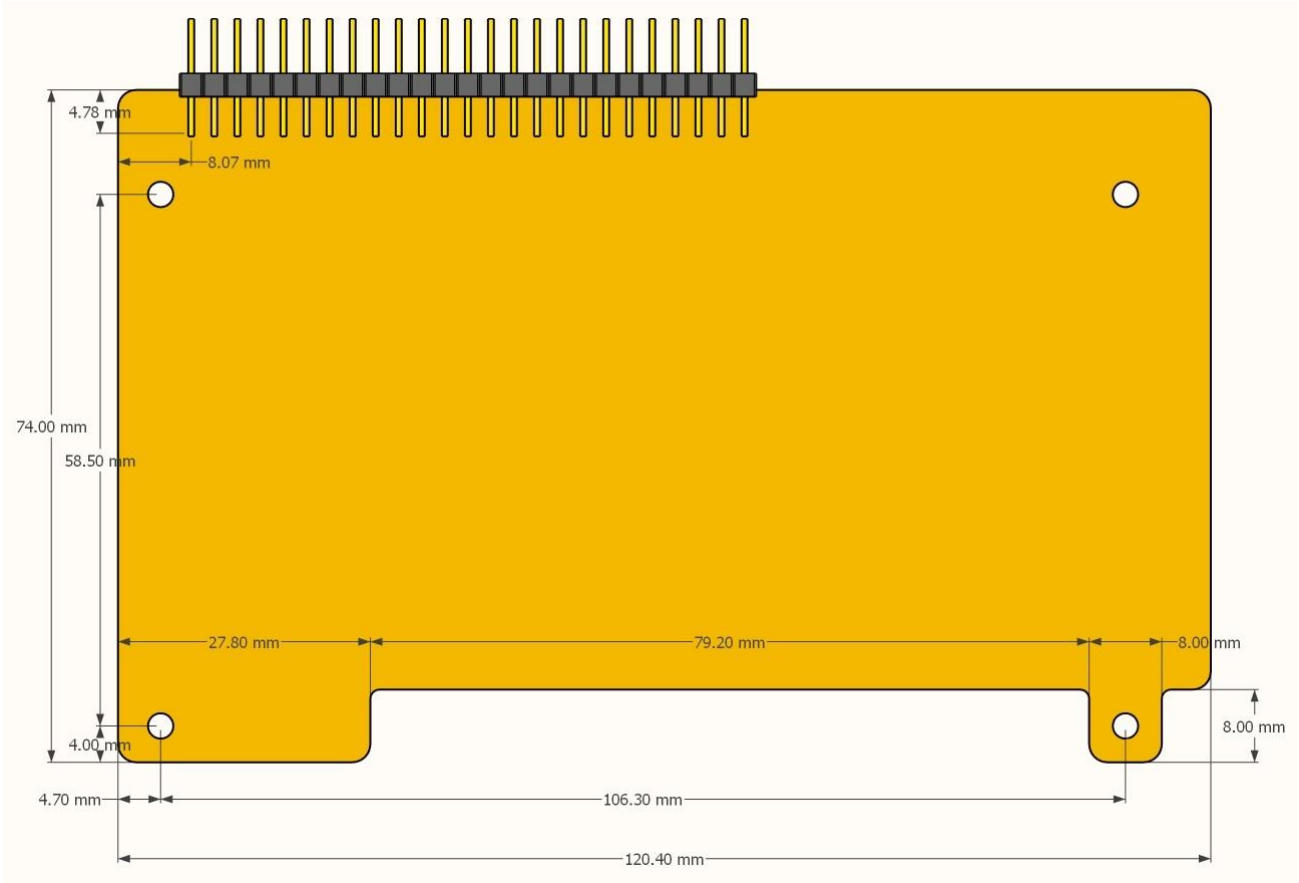
SDRAM pin assignment:

DRAM	FPGA Pin
D0	181
D1	182
D2	183
D3	184
D4	185
D5	186
D6	187
D7	188
D8	222
D9	219
D10	218
D11	217
D12	216
D13	215
D14	214
D15	213

DRAM	FPGA Pin
A0	203
A1	206
A2	207
A3	208
A4	235
A5	234
A6	233
A7	228
A8	227
A9	226
A10	202
A11	225
A12	224

DRAM	FPGA Pin
RAS#	196
CAS#	195
CS#	197
LDQM	193
UDQM	223
CLK	38
CKE	39
WE#	194
BA0	200
BA1	201

5. Internal Expansion Card Outline



6. Keyboard Controller / OSD Settings

The built-in keyboard is controlled by an MCU. Its primary functions include managing the internal keyboard and transmitting keyboard scan codes to the FPGA. Through Fn key combinations, users can control various internal devices. The following lists the Fn key functions:

- FN+1: Switch between the built-in LCD and external VGA display
- FN+3: Turn the keyboard backlight on/off
- FN+4: Switch between the built-in keyboard and external PS/2 keyboard
- FN+F3: OSD - Custom Key Scan Code Configuration (press ESC to exit)
- FN+F4: OSD-LCD menu (press ESC to exit)
- FN+F5: OSD - System Status Menu (press ESC to exit)
- FN+R: Assert the RESET Signal (Active-Low)

Active Serial Programming Interface

The OneChipBook-12 provides an ASP interface on its front panel. Users can utilize a USB Blaster programmer (supporting Active Serial mode) to program the serial EEPROM.

Active Serial Programming			
1	DCLK	2	GND
3	C_DONE	4	NC
5	n CONFIG	6	n CE
7	DATA in	8	n CS
9	DATA out	10	GND

The USB Blaster included in the package is a simplified version and is intended solely as a spare/backup unit.

(Simplified USB Blaster)

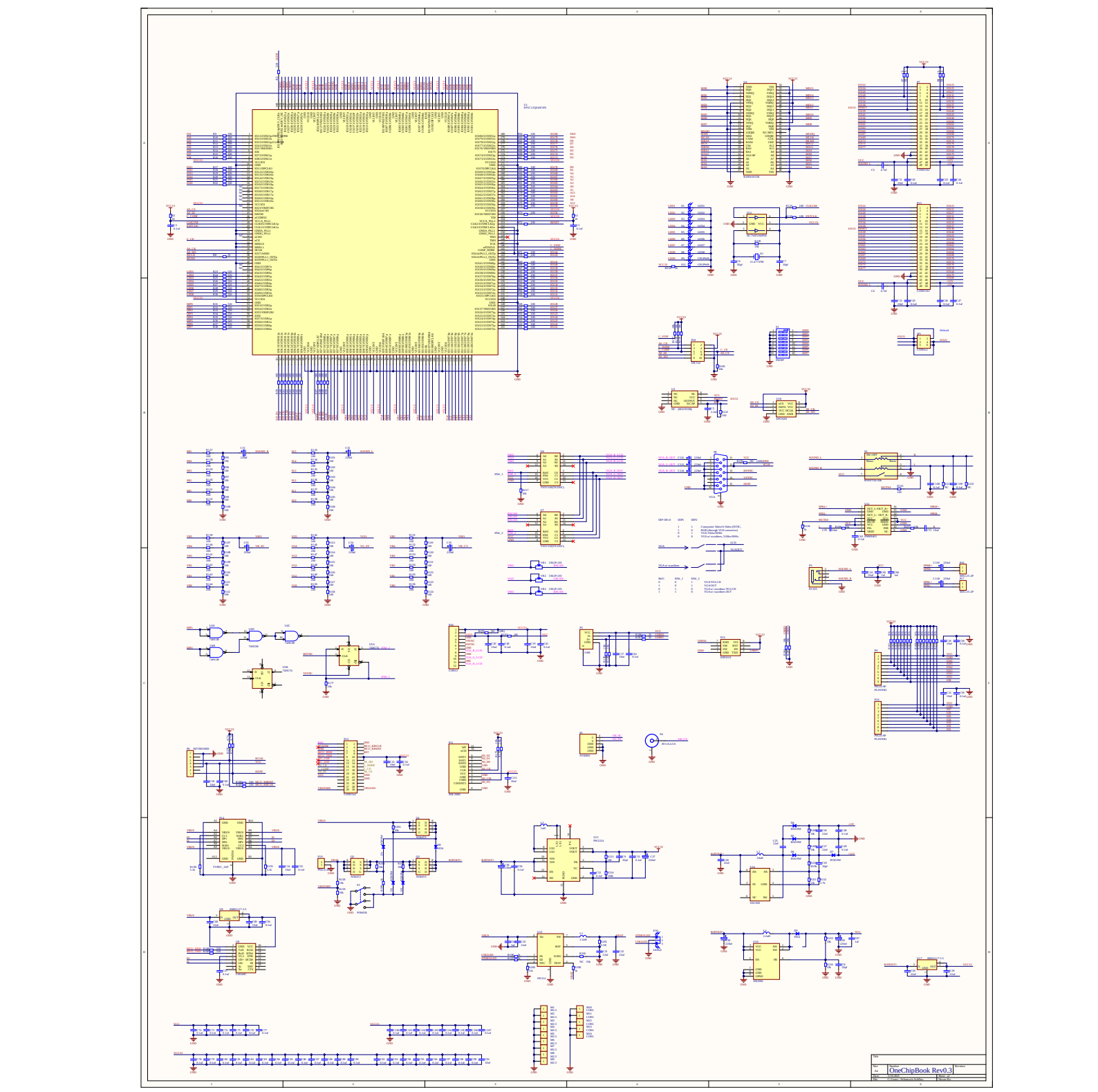
We recommend using the Intel® FPGA Download Cable.
(Ordering Part Number: PL-USB-BLASTER-RCN).

(Intel® FPGA Download Cable)

Suggested Reference Material

- Cyclone FPGA Family Data Sheet
- Quartus II Handbook Version 9.0
- Intel® FPGA Download Cable User Guide

Schematic diagram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