# Haptic Driver for ERM and LRA with Built-In Library and Smart Loop Architecture

**Check for Samples: DRV2605**

## FEATURES

- **Flexible Haptic/Vibra Driver**
  - **LRA (Linear Resonance Actuator)**
  - **ERM (Eccentric Rotating Mass)**
- **I²C Controlled Digital Playback Engine**
  - **Royalty-Free Integrated Immersion Library**
  - **Real-Time Playback Mode via I²C**
- **Smart Loop Architecture(1)**
  - **Automatic Overdrive/Braking (ERM/LRA)**
  - **Automatic Resonance Tracking (LRA)**
  - **Automatic Actuator Diagnostic (ERM/LRA)**
  - **Automatic Level Calibration (ERM/LRA)**
- **Audio To Haptics Mode**
- **Optional PWM Input with 0% to 100% Duty Cycle Control Range**
- **Optional Analog Input Control**
- **Optional Hardware Trigger Pin**
- **Efficient Output Drive**
- **Fast Start Up Time**
- **Constant Acceleration Over Supply Voltage**
- **1.8 V Compatible, VDD Tolerant Digital Pins**
- **Available in a 9-Ball, 0.5 mm Pitch WCSP**

(1) Patent pending control algorithm

## APPLICATIONS

- **Mobile Phones**
- **Tablets**
- **Touch-Enabled Devices**

## DESCRIPTION

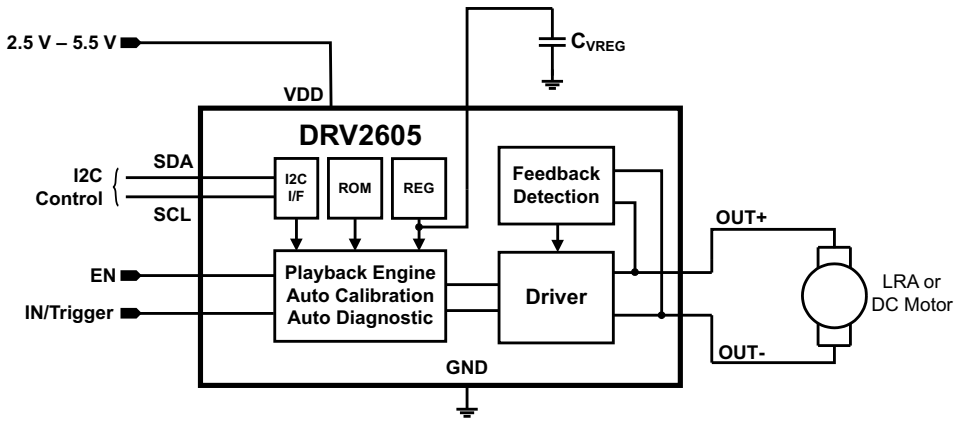
The DRV2605 is designed to give extremely flexible haptic control of ERM and LRA actuators over a shared I²C compatible bus. This relieves the host processor from ever generating pulse-width modulated (PWM) drive signals, saving both costly timer interrupts and hardware pins.

The DRV2605 gives royalty-free access to an extensive integrated library (100+ effects) from Immersion for ERM and LRA. This eliminates the need to design haptic waveforms.

Additionally, the real-time playback mode allows the host processor to bypass the library playback engine and play waveforms directly from the host via I2C.

The DRV2605 also contains a smart loop architecture, which allows effortless auto resonant drive for LRA as well as feedback-optimized ERM drive. This feedback gives automatic overdrive and braking, which creates a simplified input waveform paradigm as well as reliable motor control and consistent motor performance. The audio-to-haptics mode automatically converts an audio input signal to meaningful haptic effects.

The DRV2605 features a trinary-modulated output stage, providing greater efficiency than linear-based output drivers. The 9-ball WCSP footprint, flexible operation, and low component count make the DRV2605 the ideal choice for portable and touch-enabled vibratory and haptic applications.




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

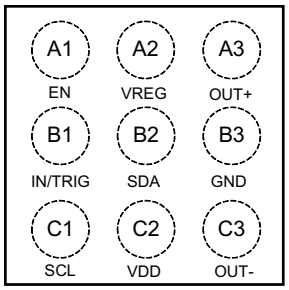
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| Device | Packaging | Symbolization |
|---|---|---|
| DRV2605YZFR | 3000 Piece Tape and Reel | 2605 |
| DRV2605YZFT | 250 Piece Tape and Reel | 2605 |

## PINOUT INFORMATION

**0.5 mm Pitch BGA (WCSP)**
**TOP VIEW**




## PIN FUNCTIONS

| PIN | | INPUT/ OUTPUT/ POWER (I/O/P) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. (WCSP) | | |
| EN | A1 | I | Device enable |
| IN/TRIG | B1 | I | Multi-mode Input. I2C selectable as PWM, Analog, or Trigger |
| SDA | B2 | I/O | $I^2C$ Data |
| SCL | C1 | I | $I^2C$ Clock |
| VREG | A2 | O | 1.8 V regulator output. 0.1 µF capacitor required |
| OUT+ | A3 | O | Positive haptic driver differential output |
| OUT– | C3 | O | Negative haptic driver differential output |
| VDD | C2 | P | Supply Input (2.5 V to 5.5 V) |
| GND | B3 | P | Supply ground |

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, $T_A$ = 25°C (unless otherwise noted)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | –0.3 V to 6.0 | V |
| $V_I$ | Input voltage | EN, SDA, SCL, IN/TRIG | –0.3 to (VDD + 0.3) | V |
| $T_A$ | Operating free-air temperature range | | –40 to 85 | °C |
| $T_J$ | Operating junction temperature range | | –40 to 150 | °C |
| $T_{stg}$ | Storage temperature range | | –65 to 150 | °C |
| | ESD Protection | HBM | 2000 | V |
| | | CDM | 500 | V |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | VALUE | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 145.2 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 0.9 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 105 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 5.1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 103.3 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | VDD | 2.5 | 5.5 | V |
| $f_{PWM}$ | PWM input frequency | IN/TRIG Pin | 10 | 250 | kHz |
| $R_L$ | Load impedance | VDD = 5.5 V | 8 | | Ω |
| $V_{IL}$ | Digital input low voltage | EN, IN/TRIG, SDA, SCL | | 0.5 | V |
| $V_{IH}$ | Digital input high voltage | EN, IN/TRIG, SDA, SCL | 1.3 | | V |
| $V_{I\text{-}ANA}$ | Input voltage (analog mode) | IN/TRIG | 0 | 1.8 | V |
| $f_{LRA}$ | LRA Frequency Range | | 50 | 300 | Hz |

## ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C, VDD = 3.6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REG}$ | | VREG | | | 1.84 | | V |
| $\|I_{IL}\|$ | Digital input low current | EN | VDD = 5.5 V , VIN = 0 V | | | 1 | µA |
| $\|I_{IH}\|$ | Digital input high current | EN | VDD = 5.5 V, VIN = VDD | | | 3.5 | µA |
| $V_{OL}$ | Digital output low voltage | SDA | $I_{OL}$ = 4 mA | | | 0.4 | V |
| $I_{SD}$ | Shut down current | $V_{EN}$ = 0 V | | | 1.75 | 4 | µA |
| $I_{SB}$ | Standby current | $V_{EN}$ = 1.8 V, STANDBY = 1 | | | 1.9 | 5 | µA |
| $I_{DDQ}$ | Quiescent current | $V_{EN}$ = 1.8 V, STANDBY = 0, no signal | | | 0.6 | 1 | mA |
| $R_{IN}$ | Input impedance | IN/TRIG to GND | | | 100 | | kΩ |
| $V_{CM-ANA}$ | IN/TRIG Common-Mode Voltage (AC Coupled) | AC_Couple = 1 | | | 0.9 | | V |
| $R_{OUT-SD}$ | Output impedance in shutdown | OUT+ to GND, OUT- to GND | | | 15 | | kΩ |
| $R_{L-SD}$ | Load impedance threshold for over-current detection | OUT+ to GND, OUT- to GND | | | 4 | | Ω |
| $t_{SU}$ | Start-up time | Time from GO or external trigger command to output signal | | | 0.7 | | ms |
| | | Time from EN high to output signal (PWM/Analog Modes) | | | 1.5 | | |
| $I_{BAT, AVG}$ | Average battery current during operation | Duty Cycle = 90%, LRA Mode, No Load | | | 2.5 | 3.25 | mA |
| | | Duty Cycle = 90%, ERM Mode, No Load | | | 2.5 | 3.25 | |
| $f_{SW}$ | PWM Output Frequency | | | 19.5 | 20.5 | 21.5 | kHz |

## TIMING REQUIREMENTS

$T_A$ = 25°C, VDD = 3.6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | Frequency, SCL | No wait states | | | 400 | kHz |
| $t_{W(H)}$ | Pulse duration, SCL high | | 0.6 | | | µs |
| $t_{W(L)}$ | Pulse duration, SCL low | | 1.3 | | | µs |
| $t_{SU1}$ | Setup time, SDA to SCL | | 100 | | | ns |
| $t_{H1}$ | Hold time, SCL to SDA | | 10 | | | ns |
| $t_{(BUF)}$ | Bus free time between stop and start condition | | 1.3 | | | µs |
| $t_{SU2}$ | Setup time, SCL to start condition | | 0.6 | | | µs |
| $t_{H2}$ | Hold time, start condition to SCL | | 0.6 | | | µs |
| $t_{SU3}$ | Setup time, SCL to stop condition | | 0.6 | | | µs |

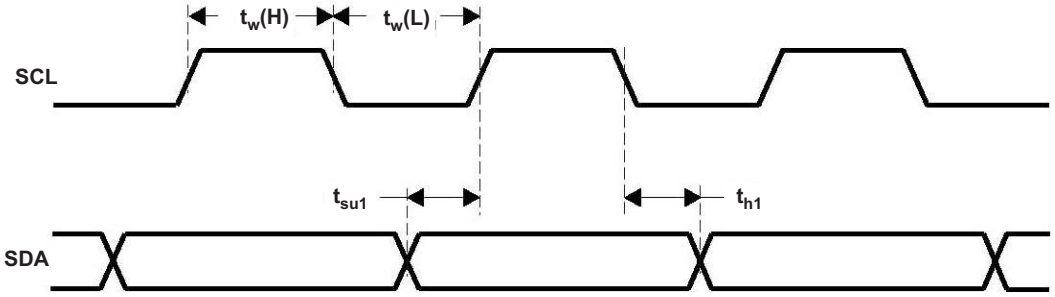



**Figure 1. SCL and SDA Timing**

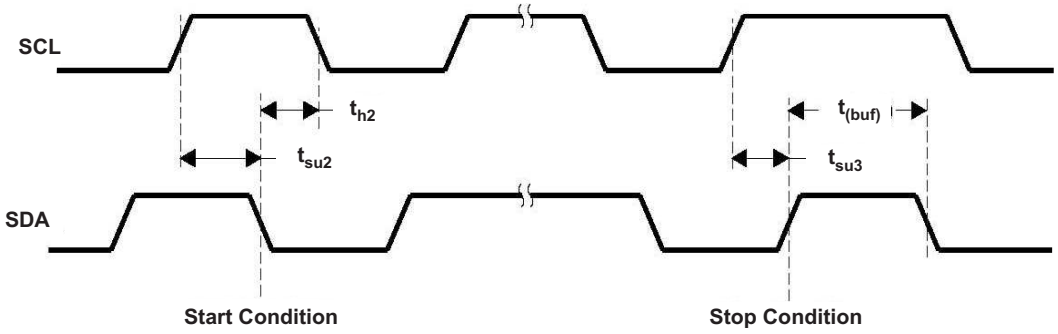



**Figure 2. Timing for Start and Stop Conditions**

## TYPICAL CHARACTERISTICS

### TEST SETUP FOR GRAPHS

To capture the graphs displayed in the this section, the following 1st order, RC filter setup was used, with the exception of "Startup Latency for ERM and LRA", which was captured without any output filter. This filter is recommended when viewing the outputs signals on an oscilloscope since output PWM modulation is present in all modes. Care must be taken that the filter does not have an effective impedance that is too low, or the closed loop and auto resonance tracking features may be affected; therefore, it is recommended that this exact filter be used for output measurement. Most oscilloscopes have an input impedance of 1 MΩ on each channel, so there is an approximate 1% loss in measured amplitude due to the voltage divider effect with the filter.

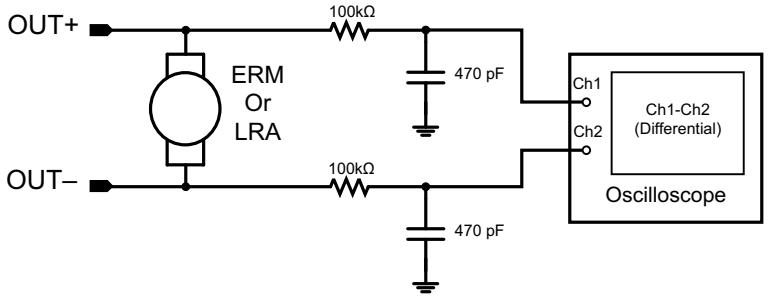



**Figure 3. Alternate Test Setup**

**Default Test Conditions:**

- VDD = 3.6 V, unless otherwise noted.
- Real actuators were used as loads for both ERM and LRA modes with exception of "Supply Voltage vs Supply Current (Full Vibration)", which used passive RL loads for test repeatability. Real actuators vary widely in supply current due to variation in back EMF voltages. Because real actuators have back EMF, the real supply current will generally be less than depicted in the graph due to reduced apparent load impedance, so the worst case current is represented in the graph.
- All ERM library waveforms taken with Library A in open loop mode
- All LRA library waveforms taken with LRA Library in closed loop mode
- All traces are 2 V/division except for the accelerometer traces
- All accelerometer traces are 0.87 g/division except for "LRA Click with and without Braking (PWM)", which is 1.74 g/division

**ERM Click (Library)**

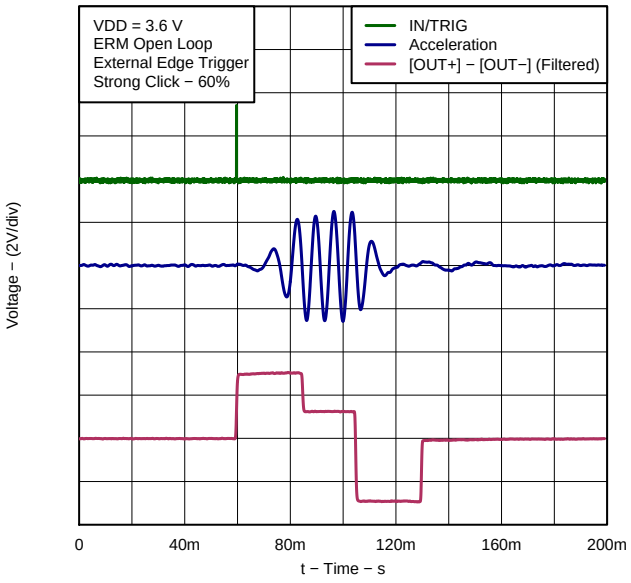



**Figure 4.**

**LRA Click (Library)**

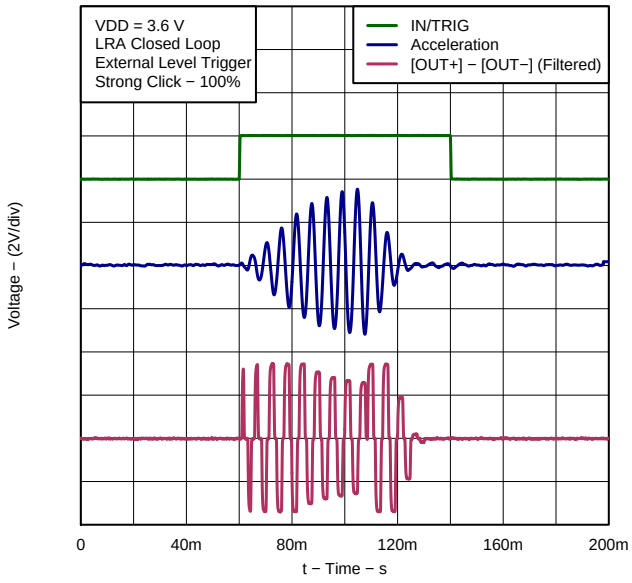



**Figure 5.**

**ERM Click-Bounce (Library)**

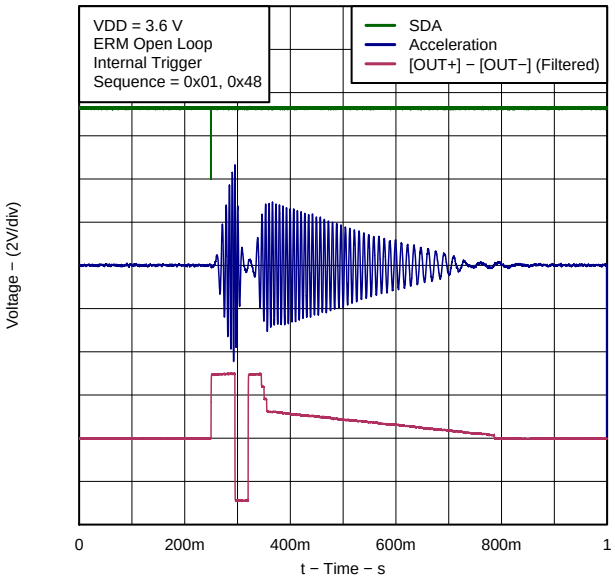



**Figure 6.**

**LRA Transition-Click (Library)**

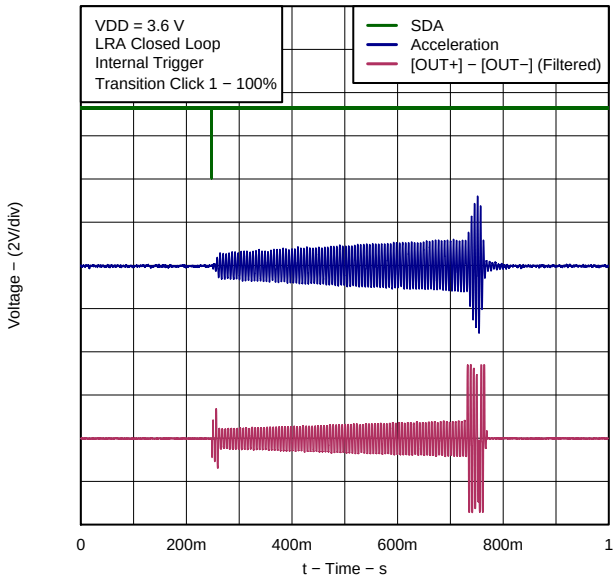



**Figure 7.**

**ERM Buzz (RTP)**

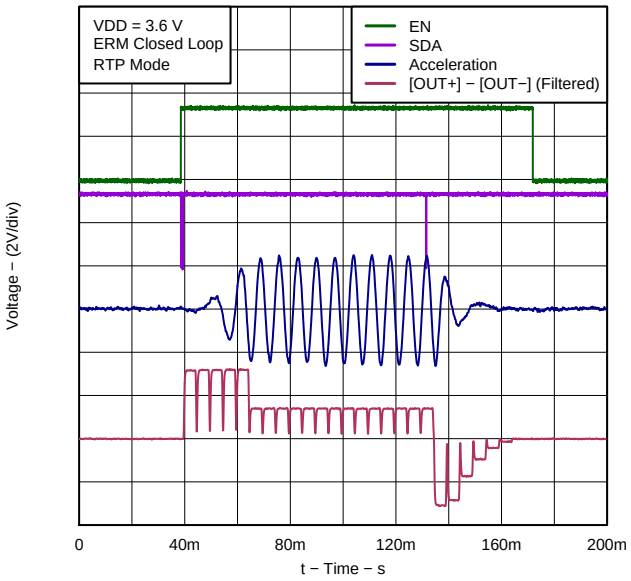



**Figure 8.**

**LRA Click with and without Braking (PWM)**

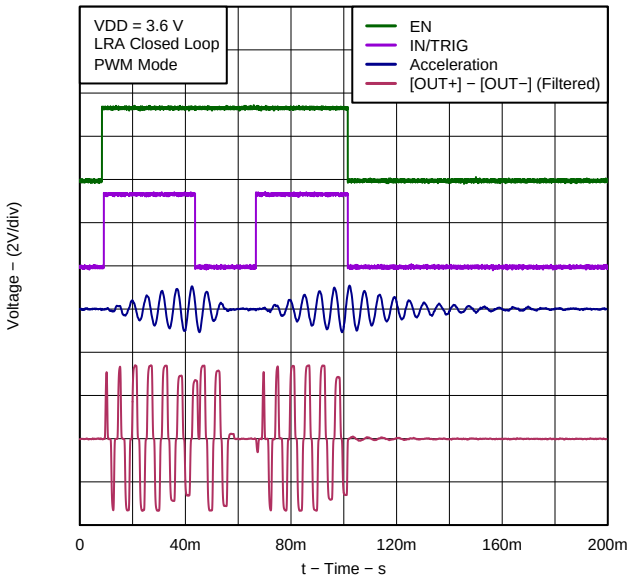



**Figure 9.**

**Startup Latency from GO for ERM and LRA**

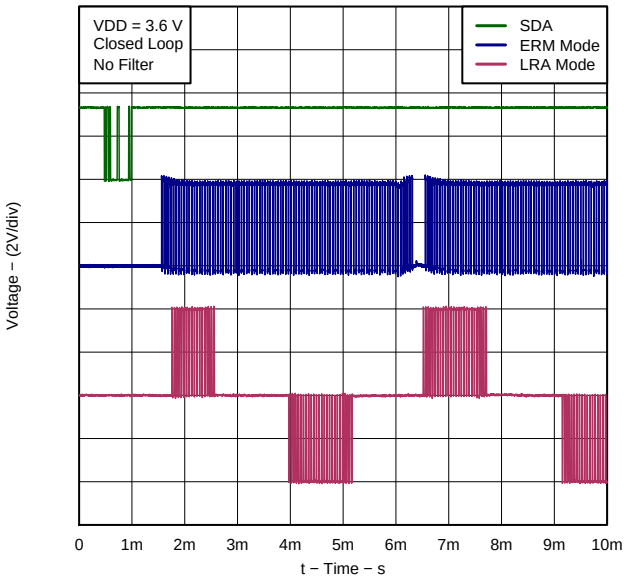



**Figure 10.**

**Supply Current Vs Supply Voltage (Full Vibration)**

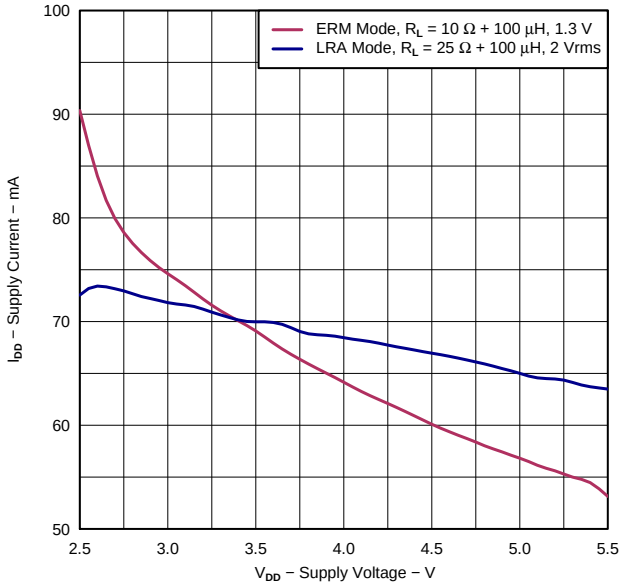



**Figure 11.**

## SYSTEM DIAGRAMS

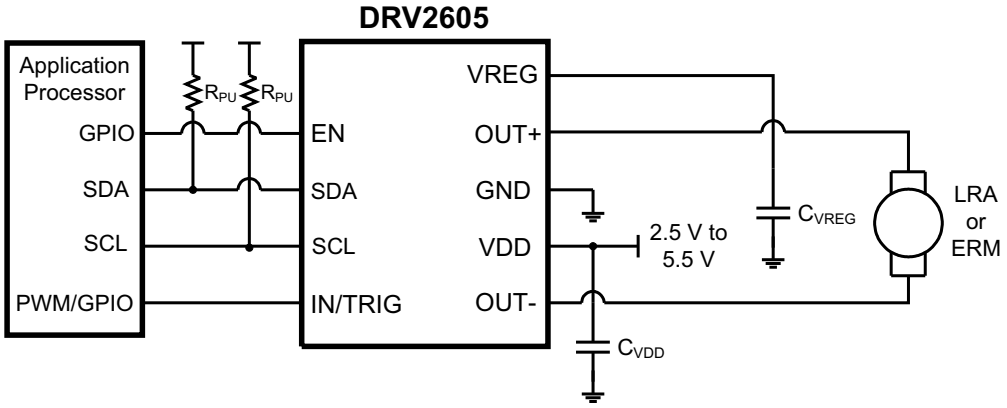



**Figure 12. I2C Control with Optional PWM Input or External Trigger**

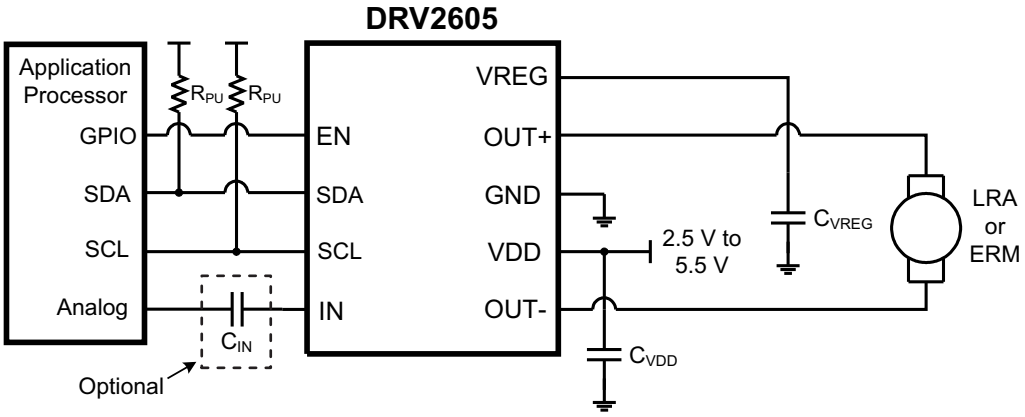



**Figure 13. I²C Control with Audio To Haptics Input and Optional AC Coupling**

## APPLICATION INFORMATION

### ECCENTRIC ROTATING MASS MOTORS (ERM)

Eccentric Rotating Mass motors, or ERMs, are typically DC-controlled motors of the bar or coin type. ERMs can be driven in the clockwise direction or counter-clockwise depending on the polarity of voltage across its two terminals. Bi-directional drive is made possible in a single-supply system by differential outputs that are capable of sourcing and sinking current. This feature helps eliminate long vibration tails which are undesirable in haptic feedback systems.

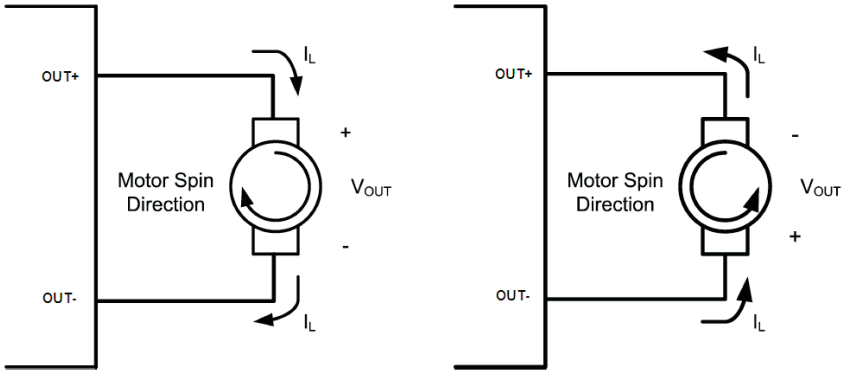



**Figure 14. Motor Spin Direction in ERM Motors**

Another common approach to driving DC motors is the concept of overdrive voltage. To overcome the inertia of the motor's mass, they are often *overdriven* for a short amount of time before returning to the motor's rated voltage to sustain the motor's rotation. Overdrive is also used to stop (or brake) a motor quickly. Reference the motor's datasheet for safe and reliable overdrive voltage and duration.

### LINEAR RESONANCE ACTUATORS (LRA)

Linear Resonant Actuators, or LRAs, vibrate optimally at their resonant frequency. LRAs have a high-Q frequency response due to which there is a rapid drop in vibration performance at offsets of 3-5 Hz from the resonant frequency. Many factors also cause a shift or drift in the resonant frequency of the actuator such as temperature, aging, the mass of the product to which the LRA is mounted, and in the case of a portable product, the manner in which it is held. Furthermore, as the actuator is driven to its maximum allowed voltage, many LRAs will shift several Hz in frequency due to mechanical compression. All of these factors make a real-time tracking auto-resonant algorithm critical when driving LRA to achieve consistent, optimized performance.

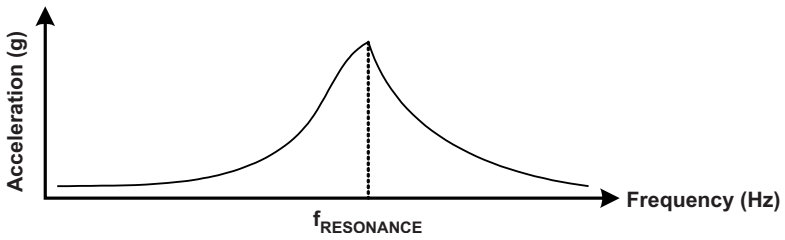



**Figure 15. Typical LRA Response**

### AUTO-RESONANCE ENGINE FOR LRA

The DRV2605 auto resonance engine tracks the resonant frequency of an LRA in real time. If the resonant frequency shifts in the middle of a waveform for any reason, the engine will track it cycle to cycle. The auto resonance engine accomplishes this by constantly monitoring the back-EMF of the actuator. Note that the auto resonance engine is not affected by the auto calibration process, which is only used for level calibration. No calibration is required for the auto resonance engine.

## OPEN LOOP OPERATION FOR LRA

The DRV2605 includes an open loop LRA drive mode for legacy systems. This mode is valid for PWM input mode only. This mode employs a fixed divider that observes the PWM signal and commutates the output drive signal at the PWM frequency divided by 128. To accomplish LRA drive, the host should drive the PWM frequency at 128 times the resonance frequency of the LRA. It is important to note that this will not benefit from the auto resonance tracking feature of the DRV2605.

## SMART LOOP ARCHITECTURE

A key feature of the DRV2605 is the smart loop architecture, which employs actuator feedback control for both ERMs and LRAs. The feedback control de-sensitizes the input waveform from the motor response behavior by providing automatic overdrive and automatic braking.

An open loop haptic system will typically drive an overdrive voltage at startup that is higher than the actuator's steady-state rated voltage to decrease the actuator's startup latency. Likewise, a braking algorithm must be employed for effective braking. When using an open loop driver, these behaviors must be contained in the input waveform data. Figure 16 illustrates how two different ERMs with different startup behaviors can both be driven optimally by the smart loop with a simple square pulse at the input. Note the smart loop works equally well for LRAs with a combination of feedback control and an auto resonance engine.

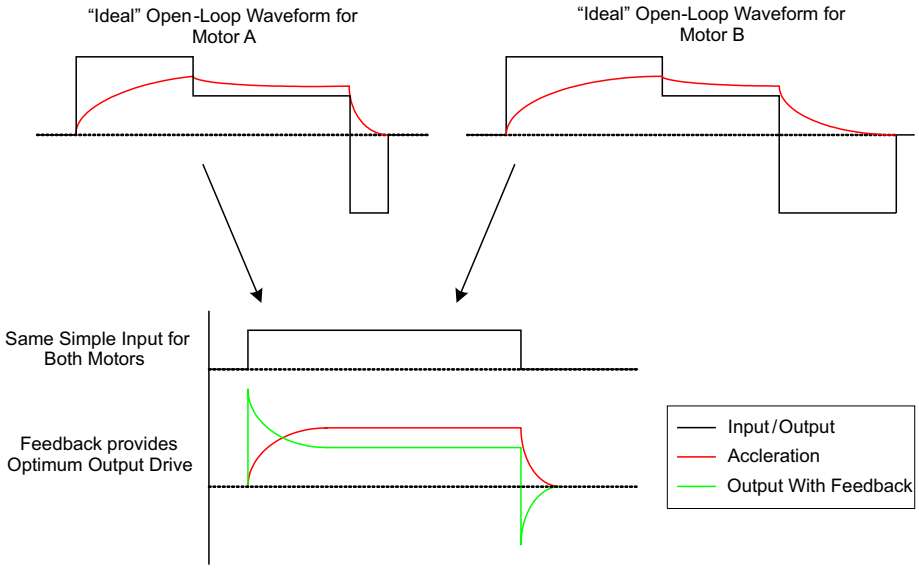



**Figure 16. Waveform Simplification with Smart Loop**

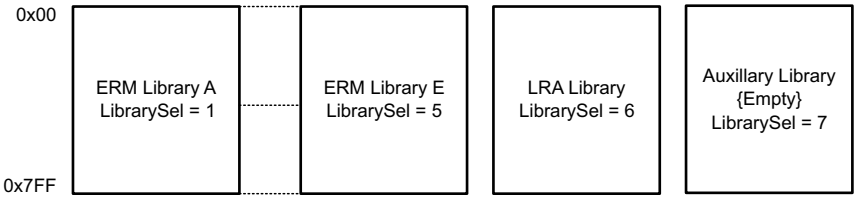
## AUTO CALIBRATION

The smart loop architecture utilizes actuator feedback by monitoring the back-EMF behavior of the actuator. The level of back-EMF can vary across actuator manufacturers due to the specific actuator construction. The auto calibration compensates for this variation and also performs scaling for the desired actuator according to the specified rated voltage and overdrive clamp register settings. After the auto calibration is performed, a 100% signal level at any of the DRV2605 input interfaces will supply the rated voltage to the actuator at steady-state. The feedback will allow the output level to go above the rated voltage level for automatic overdrive and braking, but it will not exceed the programmable overdrive clamp voltage.

See "Auto Calibration Procedure" in Device Programming section for details on performing auto calibration.

## WAVEFORM LIBRARIES

The DRV2605 has 6 internal ROM libraries designed by Immersion called TS2200. These first five libraries are specifically tuned for 5 categories of ERM motors in the open loop mode of operation. Library 6 is tuned for LRA devices. Auxiliary library 7 currently contains no information, but may be populated with other libraries in future device revisions.




## WAVEFORM SEQUENCER

The waveform sequencer (See registers 0x04 to 0x0B) is used to queue waveform library identifiers for playback. There are eight sequence registers to queue up to eight library waveforms for sequential playback. A waveform identifier is an integer value referring to the index position of a waveform in a ROM library. Playback begins at register address 0x04 when the user asserts the GO bit (Register 0x0C). When playback of that waveform ends, the waveform sequencer plays the next waveform identifier held in register 0x05, if it is non-zero. The waveform sequencer continues in this fashion until it reaches an identifier value of zero, or all eight identifiers are played (register addresses 0x04 through 0x0B), whichever comes first.

The waveform identifier range is 1 to 127. The MSB of each sequence register may be used to implement a delay between sequence waveforms. When the MSB is high, bits [6:0] are used to indicate the length of the wait time. The wait time for that step then becomes WavfrmSeq[6:0] × 10 milliseconds.

## LIBRARY PARAMETERIZATION

The ROM libraries will be augmented by the following 8-bit values in the register map. This parameterization will take place only for the ROM libraries and not for the other interfaces (e.g. PWM, RTP). The purpose of this functionality is to add “time stretching” (or time shrinking) parameters to the playback. This can be useful for customizing the entire library of waveforms for a specific actuator rise time and fall time.

ODT: Overdrive Time
SPT: Sustain Positive Time
SNT: Sustain Negative Time
BRT: Brake Time

The time values are additive offsets and are 8-bit signed values. These values are 0 offset by default. Positive values add, and negative values subtract from the “Time” value of the effect that is currently being played. The most positive value in the waveform is automatically interpreted as the overdrive time, and the most negative value in the waveform is automatically interpreted as the brake time. These time offset parameters are applied to both Voltage/Time pairs and linear ramps. For linear ramps, linear interpolation is shrunken/stretched over the two operative points for the period Time+TimeOffset, where TimeOffset is one of the time parameters listed above.

## REAL-TIME PLAYBACK (RTP) MODE

The real time playback mode is a simple, single 8-bit register interface that holds an amplitude value. It is enabled by selecting RTP Mode in the Mode register. Once real-time playback is enabled, the real-time playback register will be sent directly to the playback engine. This value is played until the user sets device in STANDBY mode or exits RTP mode. The RTP mode operates exactly like the PWM mode, except the user is entering a register value over $I^2C$ rather than a duty cycle via the input pin; therefore, any API designed to use a PWM generator in the host processor can write the data values over I2C rather than writing the data values to the host timer. This frees a timer in the host while retaining compatibility with the original software.

## MULTI-MODE INPUT PIN (IN/TRIG)

The multi-mode input pin serves four different functions:

1. PWM Input Mode
2. Analog Input Mode
3. Audio To Haptics Mode
4. Input Trigger Mode

If the IN/TRIG pin function is not needed, the pin should be tied directly to ground.

### PWM Input Option

The user may enter the PWM mode by setting Mode register value to 3 and setting the nPWM_Analog bit to 0. When in this mode, the DRV2605 accepts PWM data at the IN/TRIG pin. The DRV2605 drives the actuator continuously in this mode until the user sets the device into STANDBY mode, or enters another interface mode. The interpretation of the duty cycle information varies according to the chosen mode of operation. See “Modes Of Operation” for details.

### Analog Input Option

The user may enter the analog input mode by setting Mode register value to 3, and setting the nPWM_Analog bit to 1. When in this mode, the DRV2605 accepts an analog voltage at the IN/TRIG pin. The DRV2605 will drive the actuator continuously in this mode until the user sets the device into STANDBY mode, or enters another interface mode. The reference voltage in this mode is 1.8 V, so 1.8 V will be interpreted as a 100% input value, 0.9 V will be 50%, and 0 V will be 0%. The input value is analogous to the duty cycle percentage in PWM mode. The interpretation of these percentages varies according to the chosen mode of operation. See “Modes Of Operation” for details.

### Audio To Haptics Mode

The DRV2605 features an audio to haptics mode that converts an audio input signal into meaningful haptic effects using the Immersion "BOOMbox" technology. Audio to haptics mode adds a vibratory "bass extension" to portable devices, allowing the user to feel their audio/visual content. This is a key feature because it allows for the "haptification" of existing applications without the need for additional software drivers. Additionally, event-driven audio effects generated within an operating system can be used to automatically "haptify" a product.

To take advantage of this feature, connect the DRV2605 to a line out source as shown in Figure 13. The full-scale range of the IN/TRIG pin in the audio to haptics mode is 1.8 $V_{PP}$. The input impedance is 100 kΩ, so a resistive divider can be used if the input source is greater than 1.8 $V_{PP}$, and a 0.1 µF capacitor is recommended to AC couple the audio source and the IN/TRIG pin. For sources smaller than 1.8 $V_{PP}$, the ATH_MaxInput parameter can be used to scale down the input range. To put the device in audio to haptics mode, set Mode[2:0] = 4, and set the AC_Couple and nPWM_Analog bits to 1. See the register map for more details.

### Input Trigger Option

The user may enter the external trigger modes by setting the Mode register value to 1 or 2. A value of 1 enters Edge Mode, and a value of 2 enters Level Mode. In these modes, the IN/TRIG pin provides external trigger control of the GO bit, which allows ROM waveforms to be fired by GPIO control. This external trigger control can provide improved latencies in systems where there is significant delay between the time the effect is desired and the time a GO command can be sent over the $I^2C$ interface. Note that the effect to be triggered must already be selected to take advantage of the lower latency, so this works best for accelerating a pre-queued high-priority effect (like a button press) or for the repeated firing of the same effect (like scrolling).

### Input Trigger Options (Continued)

***Edge Mode*** – A low-to-high transition on the IN/TRIG will cause the GO bit to be set. The playback sequence indicated in the waveform sequencer will play as per normal. The user may cancel the transaction by clearing the GO bit. Another low-to-high transition while the GO bit is still high will also cancel the transaction, causing the GO bit to clear and reset. Clearing the trigger pin (high-to-low transition) does nothing, so the user may send a short pulse without knowing how long the waveform is. The pulse width should be at least 1 µs to assure detection.

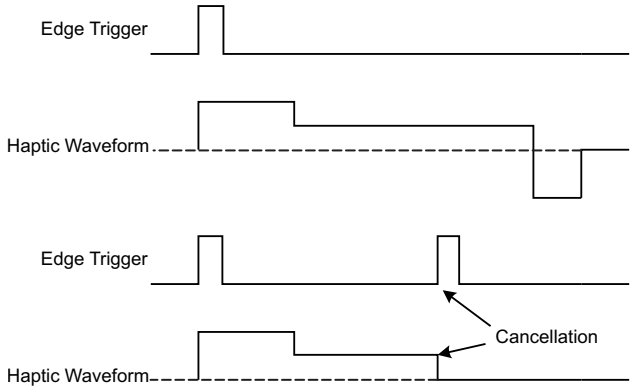



**Figure 17. Edge Trigger Mode**

***Level Mode*** – The GO bit behavior follows the IN/TRIG pin directly. When the IN/TRIG pin is high, the GO bit is high, when the trigger pin goes low, the GO bit is cleared; therefore, a falling edge will cancel the transaction. This can implement a GPIO-controlled buzz on/off controller if an appropriately long waveform is selected. The user needs to hold the IN/TRIG high for the entire duration of the waveform to complete the effect.

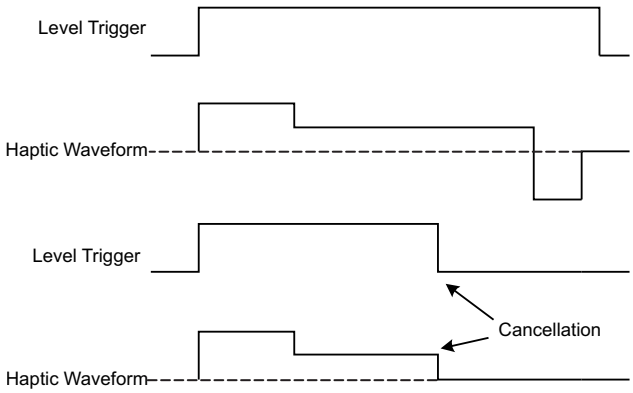



**Figure 18. Level Trigger Mode**

## DEVICE ENABLE

The EN pin of the DRV2605 is used to gate the active operation. When EN is logic high, the DRV2605 is active, and when EN is logic low, the device enters a state that is equivalent to the low-power STANDBY state. The device registers are not reset. This is particularly useful for constant source PWM/analog input modes to maintain compatibility with non-$I^2C$ device signaling. EN must be high to write $I^2C$ device registers. To completely reset the device into the power up state, set the Dev_Reset bit.

## CONSTANT VIBRATION STRENGTH

The DRV2605 PWM input uses a digital level-shifter, so as long as the input voltage meets the $V_{IH}$ and $V_{IL}$ levels, the vibration strength will remain the same even if the digital levels were to vary. The DRV2605 also features power supply feedback, so if the supply voltage drifts over time (due to battery discharge, for example), the vibration strength will remain the same so long as there is enough supply voltage to sustain the required output voltage.

## EDGE RATE CONTROL

The DRV2605 output driver implements Edge Rate Control (ERC). This ensures that the rise and fall characteristics of the output drivers do not emit levels of radiation that could interfere with other circuitry common in mobile and portable platforms. Because of ERC, no output filter, capacitors, or ferrites are necessary.

## CAPACITOR SELECTION

The DRV2605 has a switching output stage which pulls transient currents through the VDD pin. A 0.1 µF, low equivalent-series-resistance (ESR) supply bypass capacitor of the X5R or X7R type is recommended to be placed near the VDD supply pin for smooth operation of the output driver and the digital portion of the device. A similar capacitor should be placed from VREG to ground.

## MODES OF OPERATION

The DRV2605 smart loop architecture has three modes of operation. Each of these modes can be used to drive either ERM or LRA devices.

1. Open Loop Mode
2. Closed Loop Mode (Uni-Directional)
3. Closed Loop Mode (Bi-Directional)

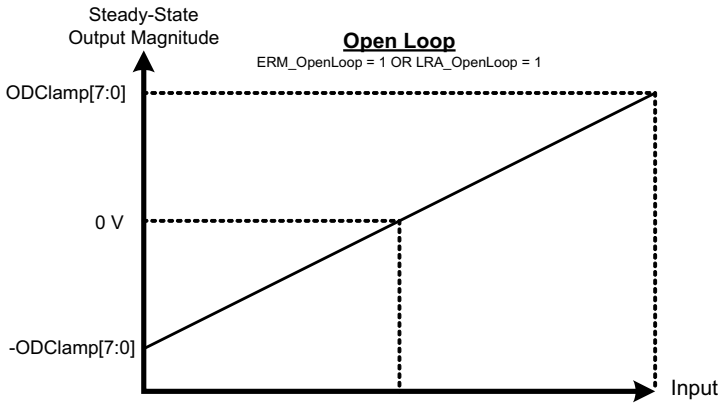
Each mode has its own advantages and disadvantages. The DRV2605 brings a new, cutting-edge actuator control with closed loop operation around the back-EMF for automatic overdrive and braking; however, some existing haptic libraries already include overdrive and braking that is embedded in the waveform data. Open loop mode is used to preserve compatibility with such systems.

The following sections show how the input data for each DRV2605 interface is translated to the output drive signal.

### Open Loop Mode

In open loop mode, the reference level for full-scale drive is set by the ODClamp[7:0] value. A mid-scale input value gives no drive signal, and less than mid-scale give a negative drive value. For ERM, a negative drive value results in counter-rotation, or braking. For LRA, this translates to a 180 degree phase shift in commutation.

The RTP mode has 8 bits of resolution over the I2C bus. The RTP data can be in either signed (2's complement) or unsigned format as defined by DataFormat_RTP.




| Input Interface | | | |
|---|---|---|---|
| PWM | 0% | 50% | 100% |
| RTP (8-bit) DataFormat_RTP = 0 | 0x81 | 0x00 | 0x7F |
| RTP (8-bit) DataFormat_RTP = 1 | 0x00 | 0x7F | 0xFF |

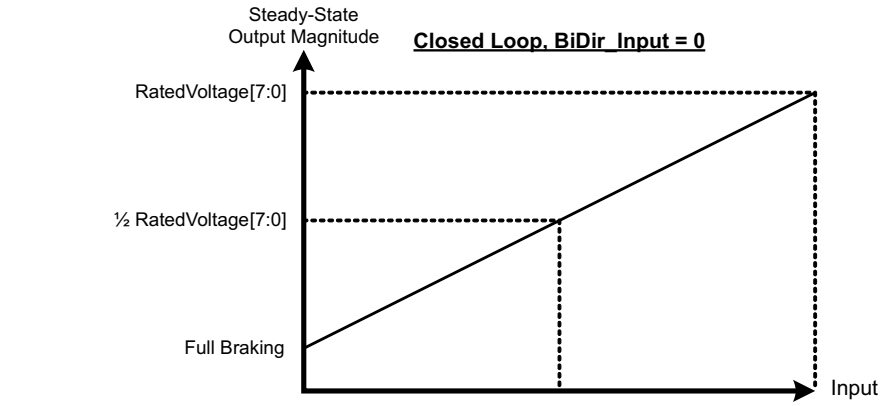
**Restrictions:** Open loop operation for LRA is only valid with the PWM interface. See "Open Loop Operation for LRA" for details. All input interfaces shown will work with ERM.

### Closed Loop Mode, Uni-Directional

In closed loop, uni-directional mode, the DRV2605 gives automatic overdrive and braking for both ERM and LRA devices. This is the most straight-forward mode to use and understand, and uses the full, 8-bit resolution of the driver. This mode gives the best performance; however, the data format is not physically compatible with the open loop mode data that may be used in some existing systems

The reference level for steady-state, full-scale drive is set by the RatedVoltage[7:0] value (once auto calibration is performed). The output voltage may momentarily exceed the rated voltage for automatic overdrive and braking, but will not exceed the ODClamp[7:0] voltage. Braking happens automatically based on the input signal when the back-EMF feedback determines that it is necessary.

Since the system is uni-directional in this mode, only unsigned data should be used. The RTP mode has 8 bits of resolution over the I2C bus. DataFormat_RTP = 0 (signed) is not recommended for this mode.




| Input Interface | | | |
|---|---|---|---|
| PWM | 0% | 50% | 100% |
| RTP (8-bit) DataFormat_RTP = 1 | 0x00 | 0x7F | 0xFF |

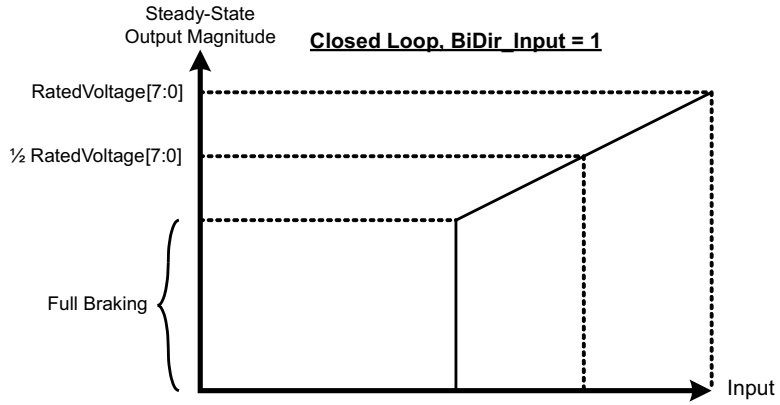
**Restrictions:** For the RTP interface, DataFormat_RTP should be set to 1 (unsigned).

### Closed Loop Mode, Bi-Directional

In closed loop, bi-directional mode, the gives automatic overdrive and braking for both ERM and LRA devices. This mode preserves compatibility with data created in open-loop signaling by keeping zero drive strength at the mid-scale value. When input values less than the mid-scale value are given, the DRV2605 will treat them the same as the mid-scale with zero drive.

The reference level for steady-state, full-scale drive is set by the RatedVoltage[7:0] value (once auto calibration is performed). The output voltage may momentarily exceed the rated voltage for automatic overdrive and braking, but will not exceed the ODClamp[7:0] voltage. Braking happens automatically based on the input signal when the back-EMF feedback determines that it is necessary. Since this mode preserves compatibility with existing/legacy dataDRV2605 formats, yet still provides closed loop benefits, it is the default configuration at power up.

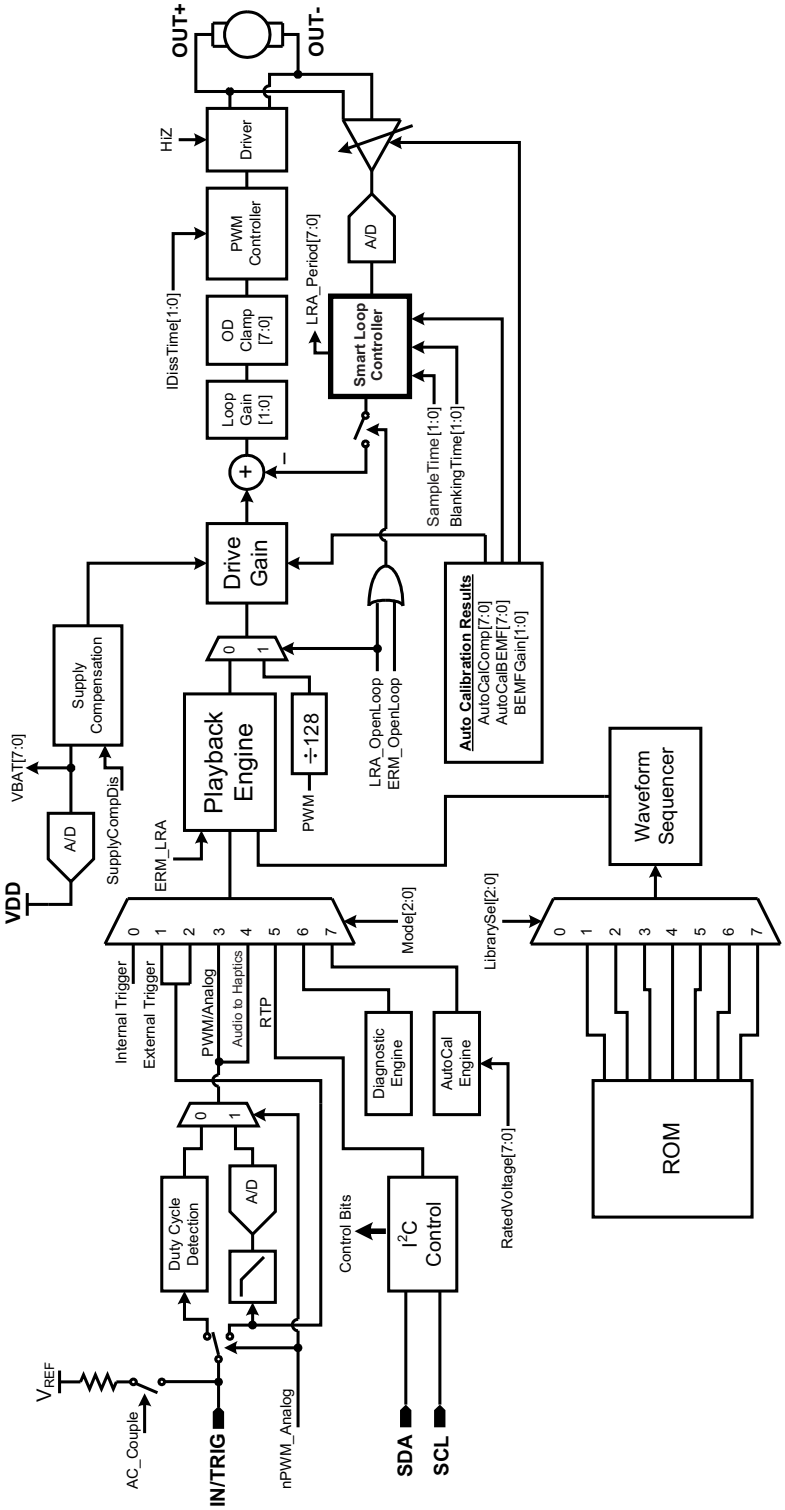
The RTP mode has 8 bits of resolution over the I2C bus. The RTP data can be in either signed (2's complement) or unsigned format as defined by DataFormat_RTP.




| Input Interface | | | | |
|---|---|---|---|---|
| PWM | 0% | 50% | 75% | 100% |
| RTP (8-bit) DataFormat_RTP = 0 | 0x81 | 0x00 | 0x3F | 0x7F |
| RTP (8-bit) DataFormat_RTP = 1 | 0x00 | 0x7F | 0xBF | 0xFF |

**Restrictions:** This mode is compatible with all DRV2605 interfaces except for TS2200 Library A (with fixed overdrive programming). Library A should only be used in open loop mode. Libraries B through E (no overdrive) may take advantage of this mode for automatic overdrive and braking.

## BLOCK DIAGRAM



## GENERAL I²C OPERATION

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The 8-bit address and data bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 19 shows a typical sequence. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with a slave device and then waits for an acknowledge condition. The slave device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 19.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Pull-up resistors between 660 Ω and 4.7 kΩ are recommended. Do not allow the SDA and SCL voltages to exceed the DRV2605 supply voltage, VDD.

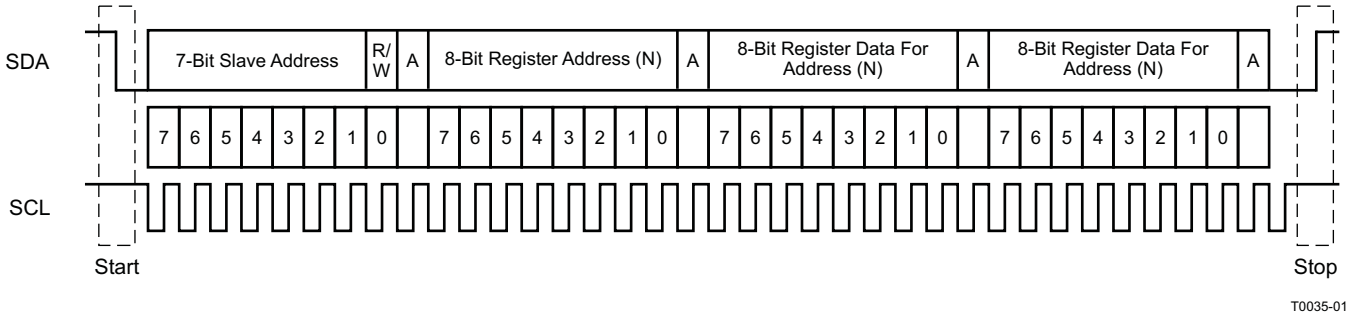



**Figure 19. Typical I²C Sequence**

The DRV2605 operates as an I²C slave 1.8 V logic thresholds, but can operate up to the VDD voltage. The device address is 0x5A (7-bit), or 1011010 in binary. This is equivalent to 0xB4 (8-bit) for writing and 0xB5 (8-bit) for reading.

## SINGLE-BYTE AND MULTIPLE-BYTE TRANSFERS

The serial control interface supports both single-byte and multiple-byte read/write operations for all registers.

During multiple-byte read operations, the DRV2605 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The DRV2605 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has taken place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

## SINGLE-BYTE WRITE

As shown in Figure 20, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the DRV2605 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to theDRV2605 internal memory address being accessed. After receiving the register byte, the DRV2605 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

The DRV2605 address is 0x5A (7-bit), or 1011010 in binary.

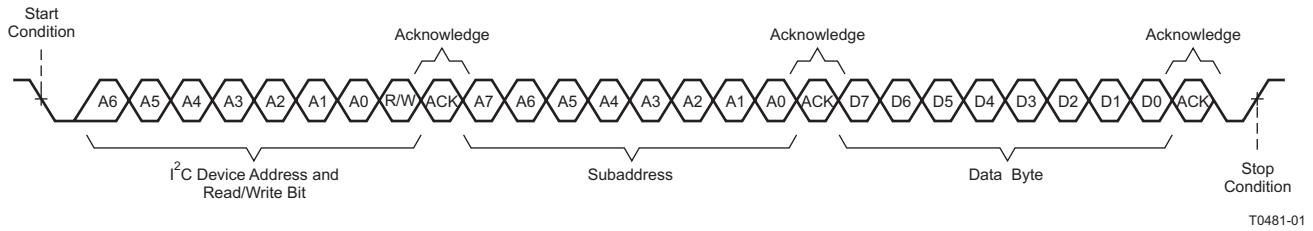



**Figure 20. Single-Byte Write Transfer**

## MULTIPLE-BYTE WRITE AND INCREMENTAL MULTIPLE-BYTE WRITE

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DRV2605 as shown in Figure 21. After receiving each data byte, the DRV2605 responds with an acknowledge bit.

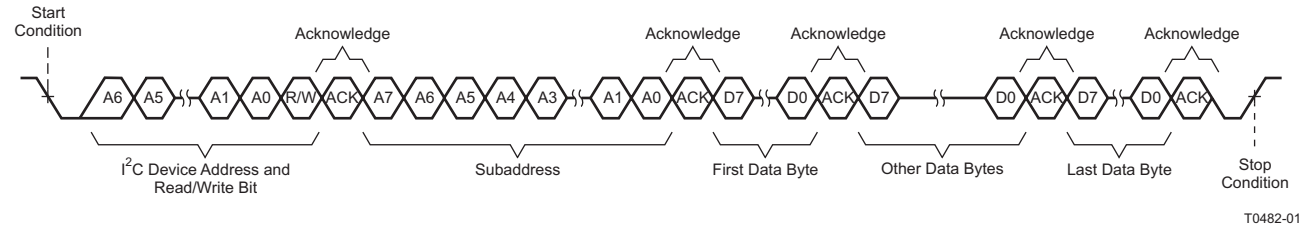



**Figure 21. Multiple-Byte Write Transfer**

## SINGLE-BYTE READ

As shown in Figure 22, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the DRV2605 address and the read/write bit, the DRV2605 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the DRV2605 issues an acknowledge bit. The master device transmits another start condition followed by the DRV2605 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the DRV2605 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

The DRV2605 address is 0x5A (7-bit), or 1011010 in binary.

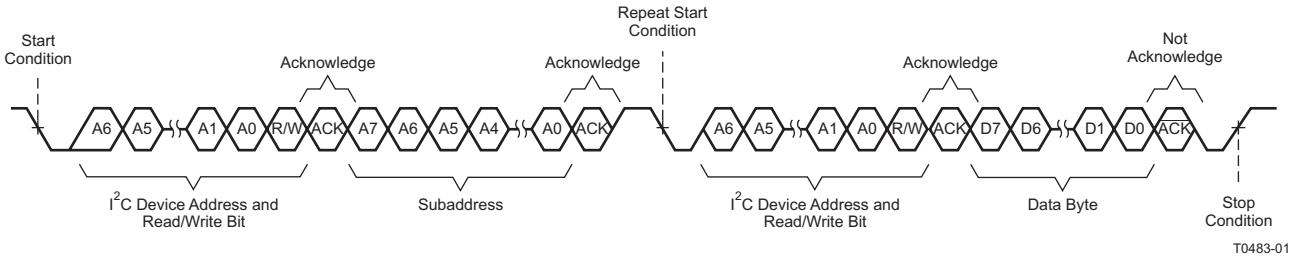



**Figure 22. Single-Byte Read Transfer**

## MULTIPLE-BYTE READ

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the DRV2605 to the master device as shown in Figure 23. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

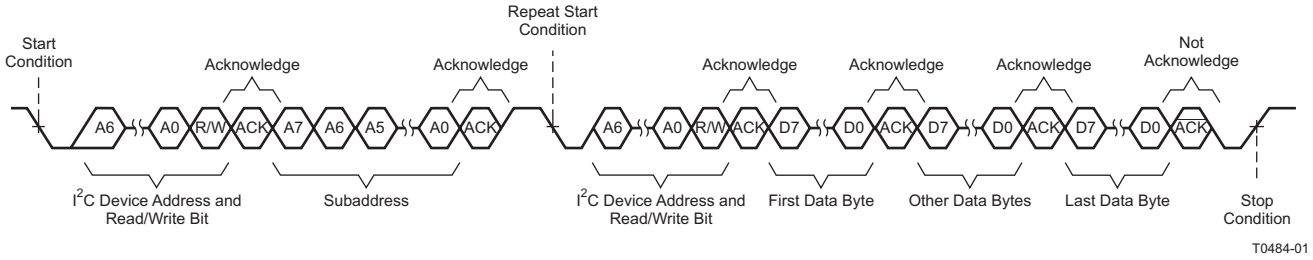



**Figure 23. Multiple-Byte Read Transfer**

## REGISTER MAP

### Table 1. Register Map Overview

| Reg# | Default | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | 0xA0 | DeviceID[2] | DeviceID[1] | DeviceID[0] | | Diag_Result | Feedback_Status | OverTemp | OC_Detect |
| 0x01 | 0x40 | Dev_Reset | STANDBY | | | | Mode[2] | Mode[1] | Mode[0] |
| 0x02 | 0x00 | RTP_Input[7] | RTP_Input[6] | RTP_Input[5] | RTP_Input[4] | RTP_Input[3] | RTP_Input[2] | RTP_Input[1] | RTP_Input[0] |
| 0x03 | 0x00 | | | | Hi_Z | | LibrarySel[2] | LibrarySel[1] | LibrarySel[0] |
| 0x04 | 0x01 | Wait1 | WavfrmSeq1[6] | WavfrmSeq1[5] | WavfrmSeq1[4] | WavfrmSeq1[3] | WavfrmSeq1[2] | WavfrmSeq1[1] | WavfrmSeq1[0] |
| 0x05 | 0x00 | Wait2 | WavfrmSeq2[6] | WavfrmSeq2[5] | WavfrmSeq2[4] | WavfrmSeq2[3] | WavfrmSeq2[2] | WavfrmSeq2[1] | WavfrmSeq2[0] |
| 0x06 | 0x00 | Wait3 | WavfrmSeq3[6] | WavfrmSeq3[5] | WavfrmSeq3[4] | WavfrmSeq3[3] | WavfrmSeq3[2] | WavfrmSeq3[1] | WavfrmSeq3[0] |
| 0x07 | 0x00 | Wait4 | WavfrmSeq4[6] | WavfrmSeq4[5] | WavfrmSeq4[4] | WavfrmSeq4[3] | WavfrmSeq4[2] | WavfrmSeq4[1] | WavfrmSeq4[0] |
| 0x08 | 0x00 | Wait5 | WavfrmSeq5[6] | WavfrmSeq5[5] | WavfrmSeq5[4] | WavfrmSeq5[3] | WavfrmSeq5[2] | WavfrmSeq5[1] | WavfrmSeq5[0] |
| 0x09 | 0x00 | Wait6 | WavfrmSeq6[6] | WavfrmSeq6[5] | WavfrmSeq6[4] | WavfrmSeq6[3] | WavfrmSeq6[2] | WavfrmSeq6[1] | WavfrmSeq6[0] |
| 0x0A | 0x00 | Wait7 | WavfrmSeq7[6] | WavfrmSeq7[5] | WavfrmSeq7[4] | WavfrmSeq7[3] | WavfrmSeq7[2] | WavfrmSeq7[1] | WavfrmSeq7[0] |
| 0x0B | 0x00 | Wait8 | WavfrmSeq8[6] | WavfrmSeq8[5] | WavfrmSeq8[4] | WavfrmSeq8[3] | WavfrmSeq8[2] | WavfrmSeq8[1] | WavfrmSeq8[0] |
| 0x0C | 0x00 | | | | | | | | GO |
| 0x0D | 0x00 | ODT[7] | ODT[6] | ODT[5] | ODT[4] | ODT[3] | ODT[2] | ODT[1] | ODT[0] |
| 0x0E | 0x00 | SPT[7] | SPT[6] | SPT[5] | SPT[4] | SPT[3] | SPT[2] | SPT[1] | SPT[0] |
| 0x0F | 0x00 | SNT[7] | SNT[6] | SNT[5] | SNT[4] | SNT[3] | SNT[2] | SNT[1] | SNT[0] |
| 0x10 | 0x00 | BRT[7] | BRT[6] | BRT[5] | BRT[4] | BRT[3] | BRT[2] | BRT[1] | BRT[0] |
| 0x11 | 0x05 | | | | | ATH_PeakTime[1] | ATH_PeakTime[0] | ATH_Filter[1] | ATH_Filter[0] |
| 0x12 | 0x19 | ATH_MinInput[7] | ATH_MinInput[6] | ATH_MinInput[5] | ATH_MinInput[4] | ATH_MinInput[3] | ATH_MinInput[2] | ATH_MinInput[1] | ATH_MinInput[0] |
| 0x13 | 0xFF | ATH_MaxInput[7] | ATH_MaxInput[6] | ATH_MaxInput[5] | ATH_MaxInput[4] | ATH_MaxInput[3] | ATH_MaxInput[2] | ATH_MaxInput[1] | ATH_MaxInput[0] |
| 0x14 | 0x19 | ATH_MinDrive[7] | ATH_MinDrive[6] | ATH_MinDrive[5] | ATH_MinDrive[4] | ATH_MinDrive[3] | ATH_MinDrive[2] | ATH_MinDrive[1] | ATH_MinDrive[0] |
| 0x15 | 0xFF | ATH_MaxDrive[7] | ATH_MaxDrive[6] | ATH_MaxDrive[5] | ATH_MaxDrive[4] | ATH_MaxDrive[3] | ATH_MaxDrive[2] | ATH_MaxDrive[1] | ATH_MaxDrive[0] |
| 0x16 | 0x3F | RatedVoltage[7] | RatedVoltage[6] | RatedVoltage[5] | RatedVoltage[4] | RatedVoltage[3] | RatedVoltage[2] | RatedVoltage[1] | RatedVoltage[0] |
| 0x17 | 0x89 | ODClamp[7] | ODClamp[6] | ODClamp[5] | ODClamp[4] | ODClamp[3] | ODClamp[2] | ODClamp[1] | ODClamp[0] |
| 0x18 | 0x0D | ACalComp[7] | ACalComp[6] | ACalComp[5] | ACalComp[4] | ACalComp[3] | ACalComp[2] | ACalComp[1] | ACalComp[0] |
| 0x19 | 0x6D | ACalBEMF[7] | ACalBEMF[6] | ACalBEMF[5] | ACalBEMF[4] | ACalBEMF[3] | ACalBEMF[2] | ACalBEMF[1] | ACalBEMF[0] |
| 0x1A | 0x36 | nERM_LRA | FBBrakeFactor[2] | FBBrakeFactor[1] | FBBrakeFactor[0] | LoopGain[1] | LoopGain[0] | BEMFGain[1] | BEMFGain[0] |
| 0x1B | 0x93 | StartupBoost | | AC_Couple | DriveTime[4] | DriveTime[3] | DriveTime[2] | DriveTime[1] | DriveTime[0] |
| 0x1C | 0xF5 | BiDir_Input | BrakeStabilizer | SampleTime[1] | SampleTime[0] | BlankingTime[1] | BlankingTime[0] | IDissTime[1] | IDissTime[0] |
| 0x1D | 0x80 | NG_Thresh[1] | NG_Thresh[0] | ERM_OpenLoop | SupplyCompDis | DataFormat_RTP | LRADriveMode | nPWM_Analog | LRA_OpenLoop |
| 0x1E | 0x20 | | | AutoCalTime[1] | AutoCalTime[0] | | OTP_Status | | OTP_Program |
| 0x21 | 0x00 | VBAT[7] | VBAT[6] | VBAT[5] | VBAT[4] | VBAT[3] | VBAT[2] | VBAT[1] | VBAT[0] |
| 0x22 | 0x00 | LRA_Period[7] | LRA_Period[6] | LRA_Period[5] | LRA_Period[4] | LRA_Period[3] | LRA_Period[2] | LRA_Period[1] | LRA_Period[0] |

### Status (Address: 0x00)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | DeviceID[2] | DeviceID[1] | DeviceID[0] | | Diag_Result | Watchdog_Status | OverTemp | OC_Detect |
| Type | RO | RO | RO | | RO | RO | RO | RO |
| Default | 1 | 0 | 1 | | 0 | 0 | 0 | 0 |

DeviceID[2:0] Device identifier. This indicates the part number to the user. The user software can ascertain the device capabilities by reading this register.

4: DRV2604 (does not contain licensed ROM library)

3: DRV2605 (contains licensed ROM library)

Diag_Result This flag stores the result of the auto calibration routine and the diagnostic routine. The flag contains the result for whichever routine was executed last. The flag clears upon read. Test result is not valid until the GO bit self-clears at the end of the routine.

Auto Calibration

0: Auto-Calibration Passed (Optimum result converged)

1: Auto-Calibration Failed (Result did not converge)

Diagnostic

0: Actuator is functioning normally

1: Actuator is not present, shorted, timing out, or giving out-of-range back-EMF

Feedback_Status Contains status for the feedback controller. This indicates when the ERM back-EMF has been zero for > ~10 ms for ERM mode, and indicates when the LRA frequency tracking has lost frequency lock in LRA mode. This bit is for debug purposes only, and may sometimes be set under normal operation when extensive braking periods are used. This bit will clear upon read.

0: Feedback controller has not timed out

1: Feedback controller has timed out

OverTemp Latching over-temperature detection flag. The device will shut itself down if it becomes too hot. Clears upon read.

0: Device is functioning normally

1: Device has exceeded the temperature threshold

OC_Detect Latching over-current detection flag. The device will shut itself down if the load impedance is below the load impedance threshold, and will periodically try to restart itself until the impedance is above the threshold.

0: No over-current event has been detected

1: Over-current even has been detected

### Mode (Address: 0x01)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | Dev_Reset | STANDBY | | | | Mode[2] | Mode[1] | Mode[0] |
| Type | R/W | R/W | | | | R/W | R/W | R/W |
| Default | 0 | 1 | | | | 0 | 0 | 0 |

Dev_Reset — Device Reset. Setting this bit performs the equivalent operation of power cycling the device. Any playback operations are immediately interrupted, and all registers are reset to their default values. The Dev_Reset bit self-clears after the reset operation is complete.

STANDBY — Software Standby Mode

0: Device Ready

1: Device in Software Standby (default)

Mode[2:0]

0: Internal Trigger (default)
Waveforms fired by setting the GO bit

1: External Trigger (Edge Mode)
A rising edge on the IN/TRIG pin sets the GO Bit. A 2nd rising edge on the IN/TRIG pin will cancel the waveform if it occurs before the GO bit has cleared.

2: External Trigger (Level Mode)
GO bit follows the state of the external trigger. A rising edge on the IN/TRIG pin sets the GO bit, and a falling edge sends a cancel. If the GO bit is already in the appropriate state, no change is effected.

3: PWM Input/Analog Input
A PWM signal is accepted at the IN/TRIG pin and used as the driving source. The device actively drives the actuator while in this mode. The user may elect to set nPWM_Analog to drive an analog signal directly into the IN/TRIG pin.

4: Audio To Haptics
An AC Coupled audio signal is accepted at the IN/TRIG pin. The device converts the audio signal into meaningful haptic vibration. The AC_Couple and nPWM_Analog bits should also be set.

5: Real-Time Playback (RTP Mode)
The device actively drives the actuator with the contents of the RTP_Data register.

6: Diagnostics
Set the device in this mode to perform a diagnostic test on the actuator. User must set the GO bit to start the test. Test is complete when the GO bit self-clears. Results are stored in the Diag_Result bit.

7: Auto Calibration
Set the device in this mode to auto calibrate for the device for the actuator. Before starting the calibration, the user must set the Rated_Voltage and ODClamp registers (0x16 and 0x17) appropriately. User must set the GO bit to start the calibration. Calibration is complete when the GO bit self-clears. Auto calibration results are stored in registers 0x18, 0x19, and 0x1A. See “Auto Calibration Procedure” for further details.

### Real-Time Playback Input (Address: 0x02)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | RTP_Input[7] | RTP_Input[6] | RTP_Input[5] | RTP_Input[4] | RTP_Input[3] | RTP_Input[2] | RTP_Input[1] | RTP_Input[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RTP_Input[7:0] This is the entry point for Real-Time Playback (RTP) data. The DRV2605 playback engine will drive the RTP_Input value to the load when Mode = 5 (RTP Mode). The RTP_Input value may be updated on the fly by the host controller to create haptic waveforms. The RTP_Input value is interpreted as signed by default, but may be set to unsigned by DataFormat_RTP. When the haptic waveform is complete, the user may park the device by setting Mode = 0, or alternatively by setting STANDBY = 1.

### Library Selection (Address: 0x03)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | | | | HiZ | | LibrarySel[2] | LibrarySel[1] | LibrarySel[0] |
| Type | | | | R/W | | R/W | R/W | R/W |
| Default | | | | 0 | | 0 | 0 | 0 |

HiZ HiZ This bit sets the output driver into a true high-impedance state. The device must be enabled to go into the high-impedance state. When in hardware shutdown or standby mode, the output drivers have 15 kΩ to ground. When HiZ is asserted, it takes effect immediately, even if a transaction is taking place.

LibrarySel[2:0] Waveform library selection value. This determines which library the playback engine goes to when the GO bit is set.

0: Empty (default)

1: TS2200 Library A – With overdrive
Designed with 3V overdrive for a 1.3V rated ERM. Open loop mode required.
Rise Time: 40 ms to 60 ms

2: TS2200 Library B – For fast, light actuators
Rise Time: 40 ms to 60 ms

3: TS2200 Library C
Rise Time: 60 ms to 80 ms

4: TS2200 Library D
Rise Time: 100 ms to 140 ms

5: TS2200 Library E
Rise Time: > 140 ms

6: LRA Library

7: Reserved

### Waveform Sequencer (Address: 0x04 to 0x0B)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | Wait | WavfrmSeq[6] | WavfrmSeq[5] | WavfrmSeq[4] | WavfrmSeq[3] | WavfrmSeq[2] | WavfrmSeq[1] | WavfrmSeq[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Wait — When this bit [7] is set, bits [6:0] are interpreted as a “wait time” in which the playback engine will idle. This is used to insert timed delays between sequentially played waveforms. Delay time is 10 ms * WavefrmSeq[6:0]. If Wait = 0, then WavfrmSeq[6:0] is interpreted as a waveform identifier for sequence playback.

WavfrmSeq[6:0] — Waveform Sequence value. Holds the waveform identifier of the waveform to be played. A waveform identifier is an integer value referring to the index position of a waveform in a ROM library. Playback begins at register address 0x04 when the user asserts the GO bit (Register 0x0C). When playback of that waveform ends, the waveform sequencer plays the next waveform identifier held in register 0x05, if it is non-zero. The waveform sequencer continues in this fashion until it reaches an identifier value of zero, or all eight identifiers are played (register addresses 0x04 through 0x0B), whichever comes first.

### GO (Address: 0x0C)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | | | | | | | | GO |
| Type | | | | | | | | R/W |
| Default | | | | | | | | 0 |

GO — Used to fire processes in the DRV2605. The process the GO bit fires is selected by the Mode[2:0] value (Register 0x01). Its primary function is to fire playback of the waveform identifiers in the waveform sequencer (Registers 0x04 to 0x0B), in which case, it can be thought of a “software trigger” for haptic waveforms. The GO bit remains high until the playback of the haptic waveform sequence is complete. Clearing the GO bit during waveform playback cancels the waveform sequence. Using one of the external trigger modes can cause the GO bit to be set or cleared by the external trigger pin. It can also be used to fire the auto calibration process or the diagnostic process.

### OverDrive Time Offset (Address: 0x0D)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | ODT[7] | ODT[6] | ODT[5] | ODT[4] | ODT[3] | ODT[2] | ODT[1] | ODT[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ODT[7:0] — Adds a time offset to the overdrive portion of the library waveforms. Some motors require more overdrive time than others, so this register allows the user to add or take away overdrive time from the library waveforms. The maximum voltage value in the library waveform is automatically determined to be the overdrive portion. This register will only be useful in open loop mode. Overdrive is automatic for closed loop mode. The offset is interpreted as two’s complement, so the time offset may be positive or negative. OverDrive Time Offset (ms) = ODT[7:0] × 5

### Sustain Time Offset, Positive (Address: 0x0E)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | SPT[7] | SPT[6] | SPT[5] | SPT[4] | SPT[3] | SPT[2] | SPT[1] | SPT[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SPT[7:0] Adds a time offset to the positive sustain portion of the library waveforms. Some motors have faster/slower response time than others, so this register allows the user to add or take away positive sustain time from the library waveforms. Any positive voltage value other than the overdrive portion will be considered a sustain positive value. The offset is interpreted as two's complement, so the time offset may be positive or negative.

Sustain Time Positive Offset (ms) = SPT[7:0] × 5

### Sustain Time Offset, Negative (Address: 0x0F)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | SNT[7] | SNT[6] | SNT[5] | SNT[4] | SNT[3] | SNT[2] | SNT[1] | SNT[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SNT[7:0] Adds a time offset to the negative sustain portion of the library waveforms. Some motors have faster/slower response time than others, so this register allows the user to add or take away negative sustain time from the library waveforms. Any negative voltage value other than the overdrive portion will be considered a sustain negative value. The offset is interpreted as two's complement, so the time offset may be positive or negative.

Sustain Time Negative Offset (ms) = SNT[7:0] × 5

### Brake Time Offset (Address: 0x10)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | BRT[7] | BRT[6] | BRT[5] | BRT[4] | BRT[3] | BRT[2] | BRT[1] | BRT[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

BRT[7:0] Adds a time offset to the braking portion of the library waveforms. Some motors require more braking time than others, so this register allows the user to add or take away brake time from the library waveforms. The most negative voltage value in the library waveform is automatically determined to be the braking portion. This register will only be useful in open loop mode. Braking is automatic for closed loop mode. The offset is interpreted as two's complement, so the time offset may be positive or negative.

## Audio To Haptics Control (Address: 0x11)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | | | | | ATH_PeakTime[1] | ATH_PeakTime[0] | ATH_Filter[1] | ATH_Filter[0] |
| Type | | | | | R/W | R/W | R/W | R/W |
| Default | | | | | 0 | 1 | 0 | 1 |

## Audio To Haptics Minimum Input Level (Address: 0x12)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | ATH_MinInput[7] | ATH_MinInput[6] | ATH_MinInput[5] | ATH_MinInput[4] | ATH_MinInput[3] | ATH_MinInput[2] | ATH_MinInput[1] | ATH_MinInput[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

## Audio To Haptics Maximum Input Level (Address: 0x13)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | ATH_MaxInput[7] | ATH_MaxInput[6] | ATH_MaxInput[5] | ATH_MaxInput[4] | ATH_MaxInput[3] | ATH_MaxInput[2] | ATH_MaxInput[1] | ATH_MaxInput[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### Audio To Haptics Minimum Output Drive (Address: 0x14)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | ATH_MinDrive[7] | ATH_MinDrive[6] | ATH_MinDrive[5] | ATH_MinDrive[4] | ATH_MinDrive[3] | ATH_MinDrive[2] | ATH_MinDrive[1] | ATH_MinDrive[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

### Audio To Haptics Maximum Output Drive (Address: 0x15)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | ATH_MaxDrive[7] | ATH_MaxDrive[6] | ATH_MaxDrive[5] | ATH_MaxDrive[4] | ATH_MaxDrive[3] | ATH_MaxDrive[2] | ATH_MaxDrive[1] | ATH_MaxDrive[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### Rated Voltage (Address: 0x16)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | RatedVoltage[7] | RatedVoltage[6] | RatedVoltage[5] | RatedVoltage[4] | RatedVoltage[3] | RatedVoltage[2] | RatedVoltage[1] | RatedVoltage[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

RatedVoltage[7:0] Sets the reference voltage for full-scale output during closed loop operation. The auto calibration routine uses this register as an input, so this register must be written with the motor's rated voltage value before calibration is performed. This register is ignored for open-loop operation, since the overdrive voltage sets the reference for that case. Any modification of this register value should be followed by calibration to set ACalBEMF appropriately.
See "Programming the Rated Voltage" for calculating the correct register value.

### Overdrive Clamp Voltage (Address: 0x17)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | ODClamp[7] | ODClamp[6] | ODClamp[5] | ODClamp[4] | ODClamp[3] | ODClamp[2] | ODClamp[1] | ODClamp[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

ODClamp[7:0] During closed loop operation, the actuator feedback lets the output voltage go above the rated voltage during the automatic overdrive and automatic braking periods. This register sets a clamp so that the automatic overdrive is bounded. This also serves as the full scale reference voltage for open loop operation.
See "Programming the Overdrive Clamp Voltage" for calculating the correct register value.

### Auto Calibration Compensation Result (Address: 0x18)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | ACalComp[7] | ACalComp[6] | ACalComp[5] | ACalComp[4] | ACalComp[3] | ACalComp[2] | ACalComp[1] | ACalComp[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

ACalComp[7:0] Contains the voltage compensation result after execution of auto calibration. This value compensates for any resistive losses in the driver. The calibration routine checks the impedance of the actuator to automatically determine an appropriate value. The auto calibration compensation result value is multiplied by the drive gain during playback.
Auto Calibration Compensation Coefficient = 1 + ACalComp[7:0] / 255

### Auto Calibration Back-EMF Result (Address: 0x19)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | ACalBEMF[7] | ACalBEMF[6] | ACalBEMF[5] | ACalBEMF[4] | ACalBEMF[3] | ACalBEMF[2] | ACalBEMF[1] | ACalBEMF[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |

ACalBEMF[7:0] Contains the rated back-EMF result after execution of auto calibration. This is the level of back-EMF voltage that the actuator gives when it is driven at its rated voltage. The DRV2605 playback engine uses this value to automatically determine the appropriate feedback gain for closed loop operation.
Auto Calibration Back-EMF (V) = (ACalBEMF[7:0] / 255) × 4.88 V / BEMFGain

### Feedback Control (Address: 0x1A)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | nERM_LRA | FBBrakeFactor[2] | FBBrakeFactor[1] | FBBrakeFactor[0] | LoopResponse[1] | LoopResponse[0] | BEMFGain[1] | BEMFGain[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

nERM_LRA — Sets the DRV2605 in ERM or LRA mode. This bit should be set prior to running auto calibration.

- 0: ERM Mode (default)
- 1: LRA Mode

FBBrakeFactor[2:0] — Selects the feedback gain ratio between braking gain and driving gain. In general, it is desirable to add additional feedback gain while braking, so that the actuator will brake as quickly as possible. Large ratios give less stable operation than lower ones. The advanced user may choose to optimize this register. Otherwise, the default value should give good performance for most actuators. This value should be set prior to running auto calibration.

- 0: 1x
- 1: 2x
- 2: 3x
- 3: 4x (default)
- 4: 6x
- 5: 8x
- 6: 16x
- 7: Braking disabled

LoopGain[1:0] — Selects a loop gain for the feedback control. This sets how fast the loop tries to make the back-EMF (and thus motor velocity) match the input signal level. Higher loop gain (faster settling) options will give less stable operation than lower loop gain (slower settling). The advanced user may choose to optimize this register. Otherwise, the default value should give good performance for most actuators. This value should be set prior to running auto calibration.

- 0: Low
- 1: Medium (default)
- 2: High
- 3: Very High

BEMFGain[1:0] — Sets the analog gain of the back-EMF amplifier. This value is interpreted differently between ERM mode and LRA mode. Auto calibration will automatically populate BEMFGain with the most appropriate value for the actuator.

ERM Mode

- 0: 0.33x
- 1: 1.0x
- 2: 1.8x (default)
- 3: 4.0x

LRA Mode

- 0: 5x
- 1:10x
- 2: 20x (default)
- 3: 30x

### Control1 (Address: 0x1B)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | StartupBoost | | AC_Couple | DriveTime[4] | DriveTime[3] | DriveTime[2] | DriveTime[1] | DriveTime[0] |
| Type | R/W | | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 1 | | 0 | 1 | 0 | 0 | 1 | 1 |

StartupBoost — Applies higher loop gain during overdrive to enhance actuator transient response.

AC_Couple — Applies a 0.9V common mode voltage to the IN/TRIG pin when an AC coupling capacitor is used. This is only useful for analog input mode. This should not be asserted for PWM mode or external trigger mode.

0: Common-mode drive disabled for DC coupling or digital inputs modes

1: Common-mode drive enabled for AC coupling

DriveTime[4:0] — LRA Mode: Sets initial “guess” for LRA drive time in LRA mode. Drive time is automatically adjusted for optimum drive on the fly; however, this register should be optimized for the approximate LRA frequence. If it is set too low, it may affect the actuator startup time. If it is set too high, it may cause instability. Optimum Drive Time (ms) ≈ 0.5 × LRA Period

Drive Time (ms) = DriveTime[4:0] × 0.1 ms + 0.5 ms

ERM Mode: Sets the sample rate for the back-EMF detection. Lower drive times cause higher peak-to-average ratios in the output signal, requiring more supply headroom. Higher drive times cause the feedback to react at a slower rate.

Drive Time (ms) = DriveTime[4:0] × 0.2 ms + 1 ms

## Control2 (Address: 0x1C)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | BiDir_Input | BrakeStabilizer | SampleTime[1] | SampleTime[0] | BlankingTime[1] | BlankingTime[0] | IDissTime[1] | IDissTime[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |

BiDir_Input — Selects the input scaling the playback engine expects.

0: Uni-directional Input Mode
Braking is automatically determined by the feedback conditions, and applied when needed. Use of this mode also recovers an additional bit of vertical resolution. This mode should only be used for closed-loop operation.
*Examples*
0% Input → No output signal
50% Input → Half-scale output signal
100% Input → Full-scale output signal

1: Bi-directional Input Mode (default)
This mode is compatible with traditional open-loop signaling, and also works well with closed-loop mode. When operating closed-loop, braking is automatically determined by the feedback conditions, and applied when needed. When operating open-loop modes, braking is only applied when the input signal is less than 50%.
***Open Loop Mode (ERM and LRA) Examples***
0% Input → Negative full-scale output signal (braking)
25% Input → Negative half-scale output signal (braking)
50% Input → No output signal
75% Input → Positive half-scale output signal
100% Input → Positive full-scale output signal

***Closed Loop Mode (ERM and LRA) Examples***
0% to 50% Input → No output signal
50% Input → No output signal
75% Input → Half-scale output signal
100% Input → Full-scale output signal

BrakeStabilizer — Reduces loop gain when braking is near completion to improve loop stability

SampleTime[1:0] — LRA Auto Resonance Sampling Time. (Advanced use only)

0: 150 µs
1: 200 µs
2: 250 µs
3: 300 µs (default)

BlankingTime[1:0] — Blanking time before the back-EMF A/D makes a conversion. (Advanced use only)

0: 15 µs (LRA), 45 µs (ERM)
1: 25 µs (LRA), 75 µs (ERM), default
2: 50 µs (LRA), 150 µs (ERM)
3: 75 µs (LRA), 225 µs (ERM)

IDissTime[1:0] — Current Dissipation Time. This is the time allowed for the current to dissipate from the actuator between PWM cycles for flyback mitigation. (Advanced use only)

0: 15 µs (LRA), 45 µs (ERM)
1: 25 µs (LRA), 75 µs (ERM), default
2: 50 µs (LRA), 150 µs (ERM)
3: 75 µs (LRA), 225 µs (ERM)

### Control3 (Address: 0x1D)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | NG_Thresh[1] | NG_Thresh[0] | ERM_OpenLoop | SupplyCompDis | DataFormat_RTP | LRADriveMode | nPWM_Analog | LRA_OpenLoop |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

NG_Thresh[1:0] Noise gate threshold for PWM and analog inputs.

0: Disabled

1: 2%

2: 4% (Default)

3: 8%

ERM_OpenLoop Selects mode of operation while in ERM mode. Closed loop operation is usually desired for its automatic overdrive and braking properties. However, many existing waveform libraries were designed for open loop operation, so open-loop operation may be required for compatibility.

0: Closed Loop (Default)

1: Open Loop

SupplyCompDis Disables supply compensation. The DRV2605 normally gives constant drive output over variation in the power supply input (VDD). In some systems supply compensation may have already been implemented upstream, so it may be useful to disable the DRV2605 supply compensation.

0: Supply Compensation Enabled (Default)

1: Supply Compensation Disabled

DataFormat_RTP Selects the input data interpretation for RTP (Real-Time Playback) mode.

0: Signed (Default)

1: Unsigned

LRADriveMode Selects the drive mode for the LRA algorithm. This determines how often the drive amplitude is updated. Updating once per cycle gives a symmetrical output signal, while updating twice per cycle gives more precise control.

0: Once per cycle (Default)

1: Twice per cycle

nPWM_Analog Selects input mode for the IN/TRIG pin when Mode[2:0] = 3.

0: PWM Input (Default)

1: Analog Input

LRA_OpenLoop Selects an Open Loop drive option for LRA Mode. When asserted, the playback engine recovers the LRA commutation frequency from the PWM input, dividing it by 128; therefore, this mode is only compatible with PWM input mode, and does not work with any other mode. The PWM input frequency must be equal to 128 times the resonant frequency of the LRA.

0: Auto Resonance Mode (Default)

1: Divide-by-128x Mode

### Auto Calibration Memory Interface (Address: 0x1E)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | | | AutoCalTime[1] | AutoCalTime[0] | | OTP_Status | | OTP_Program |
| Type | | | R/W | R/W | | RO | | R/W |
| Default | | | 1 | 0 | | 0 | | 0 |

AutoCalTime [1:0] Sets the length of the auto calibration time. This should be enough time for the motor acceleration to settle when driven at the RatedVoltage[7:0] value.

0: 150 ms (min), 350 ms (max)

1: 250 ms (min), 450 ms (max)

2: 500 ms (min), 700 ms (max), Default

3: 1000 ms (min), 1200 ms (max)

OTP_Status OTP Memory has been programmed

OTP_Program Launches the One-Time Programmable (OTP) Memory programming process, which programs the contents of register 0x16 through 0x1A into non-volatile memory. This process can only be executed one time per device. See “Auto Calibration Memory” section for further details.

### VBAT Voltage Monitor (Address: 0x21)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | VBAT[7] | VBAT[6] | VBAT[5] | VBAT[4] | VBAT[3] | VBAT[2] | VBAT[1] | VBAT[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VBAT[7:0] Gives a real time reading of the supply voltage at the VDD terminal. Device must be actively sending a waveform to take a reading.

VDD (V) = VBAT[7:0] × 5.6V / 255

### LRA Resonance Period (Address: 0x22)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | LRA_Period[7] | LRA_Period[6] | LRA_Period[5] | LRA_Period[4] | LRA_Period[3] | LRA_Period[2] | LRA_Period[1] | LRA_Period[0] |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LRA_Period[7:0] Reports the measurement of the LRA resonance period. Device must be actively sending a waveform to take a reading.

LRA Period (us) = LRA_Period[7:0] × 98.46 µs

# DEVICE PROGRAMMING

## PROGRAMMING THE RATED VOLTAGE

The RatedVoltage[7:0] value (Register 0x16) is used to set the full scale voltage for the closed-loop drive modes. The auto calibration routine uses this register as an input, so this register must be written with the motor's rated voltage value before calibration is performed. ***This register is ignored for open-loop operation***, since the overdrive voltage sets the reference for that case. Any modification of this register value should be followed by calibration to set ACalBEMF appropriately. See "Modes Of Operation" for more details on how this value is used.

### ERM Mode (Closed Loop)

Equation 1 gives the average steady-state voltage when a full-scale input signal is provided.

$$V_{AVG} = \text{Rated Voltage } [7:0] \frac{5.36\ V}{255} \tag{1}$$

### LRA Mode (Closed Loop)

Equation 2 gives the average of the absolute value of the LRA drive voltage when driven to steady state with a full-scale input signal.

$$V_{AVG\_ABS} = \text{Rated Voltage } [7:0] \frac{5.28\ V}{255} \tag{2}$$

And Equation 3 converts the average of the absolute value obtained in Equation 2 to the steady-state RMS voltage.

$$V_{RMS} = \frac{1}{\sqrt{1 - (4\,\text{SampleTime} + 300\,\mu s)\, f_{LRA}}} V_{AVG\_ABS} \tag{3}$$

*Default Values:*
SampleTime = 300 µs
$f_{LRA}$ = 175 Hz
$V_{RMS}$ = 1.16 $V_{AVG\_ABS}$ (with default values)

## PROGRAMMING THE OVERDRIVE CLAMP VOLTAGE

During closed loop operation, the actuator feedback lets the output voltage go above the rated voltage during the automatic overdrive and automatic braking periods. The ODClamp[7:0] value (Register 0x17) sets a clamp so that the automatic overdrive is bounded. This also serves as the full scale reference voltage for open loop operation. The ODClamp[7:0] value always represents the *peak voltage* that is allowed, regardless of the mode. Note that if the supply voltage (VDD) is less than the overdrive clamp voltage, the output driver will not be able to reach the clamp voltage value because the output voltage cannot exceed the supply voltage. Also note that if the rated voltage exceeds the overdrive clamp voltage, the overdrive clamp voltage will supercede.

### LRA Mode (Closed Loop) and ERM Mode (Open Loop)

Equation 4 is the peak voltage allowed during all modes of operation.

$$V_{OD} = \text{ODClamp}[7:0] \frac{5.6\ V}{255} \tag{4}$$

### ERM Mode (Closed Loop)

Although Equation 5 gives the peak voltage for the overdrive clamp, it is desirable in ERM mode to know the *average* voltage obtained when clamped. The closed loop mode periodically samples the actuator back EMF. During this time, the driver is not applying voltage to the actuator. To achieve equivalent performance between the open loop and closed loop modes, it is useful to relate the peak clamp voltage to the average voltage. This relationship is given by Equation 6.

$$V_{PEAK} = \text{ODClamp}[7:0] \frac{5.44\ V}{255} \tag{5}$$

$$V_{AVG} = \frac{(\text{DriveTime} - 300\mu s)}{\text{DriveTime} + \text{IDissTime} + \text{BlankingTime}} V_{PEAK} \tag{6}$$

*Default Values:*
DriveTime = 4.8 ms
IDissTime = BlankingTime = 75 µs
$V_{AVG}$ = 0.91 $V_{PEAK}$ (with default values)

### LRA Mode (Open Loop)

The ODClamp[7:0] value sets the peak value when open loop LRA mode is used. Please note that LRA Open Loop Mode can only be used with PWM inputs.

$$V_{PEAK} = \text{ODClamp}[7:0] \frac{5.44V}{255} \tag{7}$$

The $V_{RMS}$ value can be calculated from the peak value using the following equation:

$$V_{RMS} = V_{PEAK} \sqrt{1 - (800\ \mu s) f_{LRA}} \tag{8}$$

## AUTO CALIBRATION PROCEDURE

1. Determine parameters for selected actuator
   (a) Type: ERM or LRA
   (b) Rated voltage
   (c) Allowed overdrive voltage
2. Apply the supply voltage to the DRV2605. The supply voltage should allow adequate drive voltage for the selected actuator.
3. Write a value of 0x07 to register 0x01. This will take the DRV2605 out of STANDBY and place the Mode[2:0] bits in auto calibration mode.
4. Write the nERM_LRA, FBBrakeFactor and LoopResponse values to register 0x1A. The BEMFGain bits will be populated automatically by the auto calibration algorithm. Default values for register 0x1A that work for most actuators are 0x24 for ERM and 0xA4 for LRA.
5. Write the actuator rated voltage to register 0x16 using the formula:
   See "Programming the Rated Voltage" for calculating the correct register value.
6. Write the actuator overdrive clamp voltage to register 0x17 using the formula:
   See "Programming the Overdrive Clamp Voltage" for calculating the correct register value.
7. Set the GO bit to start the auto calibration process (Write a value of 0x01 to register 0x0C). When auto calibration is complete, the GO bit will self-clear. The auto calibration duration can be adjusted with AutoCalTime[1:0]. The auto calibration results will be written to ACalComp[7:0], ACalBEMF[7:0], and BEMFGain[1:0].
8. Check the status of the Diag_Result bit to ensure that the auto calibration routine completed without faults.
9. Evaluate system performance with the auto calibrated settings. Note that the evaluation should be done in the final assembly of the product, as this can affect actuator performance/behavior. If any adjustment is needed, steps 4 through 8 can be repeated. If the performance is satisfactory, the user may choose to do any of the following:
   (a) Repeat the calibration process upon subsequent power ups.
   (b) Store the auto calibration results in host processor memory and rewrite them to the DRV2605 upon subsequent power ups. The DRV2605 remembers these settings when in STANDBY mode or when EN is low.
   (c) Permanently program the results in non-volatile, on-chip auto calibration memory. Even when the DRV2605 is power cycled, it will remember the auto calibration settings. This procedure is described in the following section.

## AUTO CALIBRATION MEMORY

The DRV2605 contains non-volatile, on-chip, One-Time Programmable (OTP) auto calibration memory for the auto calibration specific parameters. Once written, the DRV2605 remembers the device settings in registers 0x16 through 0x1A even after power cycling. This allows the user to account for small variations in actuator manufacturability from unit to unit as well as shorten the device initialization process for product specific parameters such as actuator type, actuator rated voltage, etc. An additional benefit is that the DRV2605 memory can be customized at the product test level without driving changes in the product software.

To permanently program the auto calibration memory, use the following steps:

1. Complete the auto calibration process described in the “Auto Calibration Procedure”. Ensure that the performance is satisfactory, since this procedure is permanent and can only be completed once.
2. Ensure that the supply voltage (VDD) is between 4.0 V and 4.4 V. This voltage is required for the non-volatile memory to program properly.
3. Set the OTP_Launch bit by writing a value of 0x01 to register 0x1E. Once the OTP memory has been written, the OTP_Status bit will read 1.
4. Reset the device by power cycling or setting Dev_Reset. Read register 0x16 to 0x1A to ensure that the programmed values were retained.

## TYPICAL USAGE EXAMPLES

### Initialization Procedure

1. After power up, wait at least 250 µs before the DRV2605 will accept $I^2C$ commands.
2. Assert the EN pin (logic high). The EN pin may be asserted any time during or after the 250 µs wait period.
3. Write the MODE register (address 0x01) to value 0x00 to take the device out of STANDBY mode.
4. If the non-volatile, auto-calibration memory has been programmed as described in the previous section, skip to step 6.
5. Perform the steps as described in "Auto Calibration Procedure". Alternatively, rewrite the results from a previous calibration. Registers that should be written in this step are Rated Voltage (0x16), Overdrive Clamp Voltage (0x17), Auto Calibration Compensation (0x18), Auto Calibration Back-EMF (0x19), and Feedback Control (0x1A). Note: If only Open Loop operation is used, the Auto Calibration Back-EMF and Feedback Control [6:0] need not be written. Feedback Control [7] should be written to select ERM or LRA mode.
6. If using the embedded ROM library, write the Library Selection register (address 0x03) to choose a library.
7. The default setup is closed-loop, bi-directional mode. To use other modes and features, write Control1 (0x1B), Control2 (0x1C), and Control3 (0x1D) as necessary. Open Loop operation is recommended for ERM mode when using the ROM libraries. See Register Map and "Modes of Operation" in the application information for details.
8. Put the device in STANDBY or de-assert the EN pin, whichever is most convenient. Both are low power modes. The user may select the desired MODE (address 0x01) at the same time the STANDBY bit is set.

### Play a Waveform or Waveform Sequence from ROM Waveform Memory

1. Initialize the device as shown in "Initialization Procedure".
2. Assert the EN pin (active high) if it was previously de-asserted.
3. Select the desired MODE value of 0 (internal trigger), 1 (external edge trigger), or 2 (external level trigger) in the MODE register (address 0x01). If the STANDBY bit was previously asserted, it should be de-asserted (logic low) at this time. If register 0x01 already holds the desired value and the STANDBY bit is low, this step may be skipped.
4. Select the waveform index to be played and write it to address 0x04. Alternatively, a sequence of waveform indices may be written to register 0x04 through 0x0B. See "Waveform Sequencer" in the application information for details.
5. If using the internal trigger mode, set the GO bit (address 0x0C, bit 0) to fire the effect or sequence of effects. If using an external trigger mode, send an appropriate trigger pulse to the IN/TRIG pin. See "Input Trigger Options" in the application information for details.
6. If desired, the user may repeat step 5 to fire the effect or sequence again.
7. Put the device in low power mode by de-asserting EN or setting the STANDBY bit.

### Play a Real-Time Playback (RTP) Waveform

1. Initialize the device as shown in "Initialization Procedure".
2. Assert the EN pin (active high) if it was previously de-asserted.
3. Set the MODE value to 5 (RTP Mode) at address 0x01. If the STANDBY bit was previously asserted, it should be de-asserted (logic low) at this time. If register 0x01 already holds the desired value and the STANDBY bit is low, this step may be skipped.
4. Write the desired drive amplitude to the Real Time Playback Input register (address 0x02). See "Modes of Operation" for drive amplitude scaling.
5. Once the desired sequence of drive amplitudes is complete, put the device in low power mode by de-asserting EN or setting the STANDBY bit.

### Play a PWM or Analog Input Waveform

1. Initialize the device as shown in "Initialization Procedure".
2. Assert the EN pin (active high) if it was previously de-asserted.
3. Set the MODE value to 3 (PWM/Analog Mode) at address 0x01. If the STANDBY bit was previously asserted, it should be de-asserted (logic low) at this time. If register 0x01 already holds the desired value and the STANDBY bit is low, this step may be skipped.
4. Select the input mode (PWM or Analog) in the Control3 register (address 0x1D). If this was chosen during the initialization procedure, this step may be skipped.
5. Send the desired PWM/Analog input waveform sequence from the external source. See "Modes of Operation" for drive amplitude scaling.
6. Once the desired drive sequence is complete, put the device in low power mode by de-asserting EN or setting the STANDBY bit.

## WAVEFORM LIBRARY EFFECTS LIST

| Effect ID# | Waveform Name | Effect ID# | Waveform Name | Effect ID# | Waveform Name |
|---|---|---|---|---|---|
| 1 | Strong Click - 100% | 42 | Long Double Sharp Click Medium 2 – 80% | 83 | Transition Ramp Up Long Smooth 2 – 0 to 100% |
| 2 | Strong Click - 60% | 43 | Long Double Sharp Click Medium 3 – 60% | 84 | Transition Ramp Up Medium Smooth 1 – 0 to 100% |
| 3 | Strong Click - 30% | 44 | Long Double Sharp Tick 1 – 100% | 85 | Transition Ramp Up Medium Smooth 2 – 0 to 100% |
| 4 | Sharp Click - 100% | 45 | Long Double Sharp Tick 2 – 80% | 86 | Transition Ramp Up Short Smooth 1 – 0 to 100% |
| 5 | Sharp Click - 60% | 46 | Long Double Sharp Tick 3 – 60% | 87 | Transition Ramp Up Short Smooth 2 – 0 to 100% |
| 6 | Sharp Click - 30% | 47 | Buzz 1 – 100% | 88 | Transition Ramp Up Long Sharp 1 – 0 to 100% |
| 7 | Soft Bump - 100% | 48 | Buzz 2 – 80% | 89 | Transition Ramp Up Long Sharp 2 – 0 to 100% |
| 8 | Soft Bump - 60% | 49 | Buzz 3 – 60% | 90 | Transition Ramp Up Medium Sharp 1 – 0 to 100% |
| 9 | Soft Bump - 30% | 50 | Buzz 4 – 40% | 91 | Transition Ramp Up Medium Sharp 2 – 0 to 100% |
| 10 | Double Click - 100% | 51 | Buzz 5 – 20% | 92 | Transition Ramp Up Short Sharp 1 – 0 to 100% |
| 11 | Double Click - 60% | 52 | Pulsing Strong 1 – 100% | 93 | Transition Ramp Up Short Sharp 2 – 0 to 100% |
| 12 | Triple Click - 100% | 53 | Pulsing Strong 2 – 60% | 94 | Transition Ramp Down Long Smooth 1 – 50 to 0% |
| 13 | Soft Fuzz - 60% | 54 | Pulsing Medium 1 – 100% | 95 | Transition Ramp Down Long Smooth 2 – 50 to 0% |
| 14 | Strong Buzz - 100% | 55 | Pulsing Medium 2 – 60% | 96 | Transition Ramp Down Medium Smooth 1 – 50 to 0% |
| 15 | 750 ms Alert 100% | 56 | Pulsing Sharp 1 – 100% | 97 | Transition Ramp Down Medium Smooth 2 – 50 to 0% |
| 16 | 1000 ms Alert 100% | 57 | Pulsing Sharp 2 – 60% | 98 | Transition Ramp Down Short Smooth 1 – 50 to 0% |
| 17 | Strong Click 1 - 100% | 58 | Transition Click 1 – 100% | 99 | Transition Ramp Down Short Smooth 2 – 50 to 0% |
| 18 | Strong Click 2 - 80% | 59 | Transition Click 2 – 80% | 100 | Transition Ramp Down Long Sharp 1 – 50 to 0% |
| 19 | Strong Click 3 - 60% | 60 | Transition Click 3 – 60% | 101 | Transition Ramp Down Long Sharp 2 – 50 to 0% |
| 20 | Strong Click 4 - 30% | 61 | Transition Click 4 – 40% | 102 | Transition Ramp Down Medium Sharp 1 – 50 to 0% |
| 21 | Medium Click 1 - 100% | 62 | Transition Click 5 – 20% | 103 | Transition Ramp Down Medium Sharp 2 – 50 to 0% |
| 22 | Medium Click 2 - 80% | 63 | Transition Click 6 – 10% | 104 | Transition Ramp Down Short Sharp 1 – 50 to 0% |
| 23 | Medium Click 3 - 60% | 64 | Transition Hum 1 – 100% | 105 | Transition Ramp Down Short Sharp 2 – 50 to 0% |
| 24 | Sharp Tick 1 - 100% | 65 | Transition Hum 2 – 80% | 106 | Transition Ramp Up Long Smooth 1 – 0 to 50% |
| 25 | Sharp Tick 2 - 80% | 66 | Transition Hum 3 – 60% | 107 | Transition Ramp Up Long Smooth 2 – 0 to 50% |
| 26 | Sharp Tick 3 – 60% | 67 | Transition Hum 4 – 40% | 108 | Transition Ramp Up Medium Smooth 1 – 0 to 50% |
| 27 | Short Double Click Strong 1 – 100% | 68 | Transition Hum 5 – 20% | 109 | Transition Ramp Up Medium Smooth 2 – 0 to 50% |
| 28 | Short Double Click Strong 2 – 80% | 69 | Transition Hum 6 – 10% | 110 | Transition Ramp Up Short Smooth 1 – 0 to 50% |
| 29 | Short Double Click Strong 3 – 60% | 70 | Transition Ramp Down Long Smooth 1 – 100 to 0% | 111 | Transition Ramp Up Short Smooth 2 – 0 to 50% |
| 30 | Short Double Click Strong 4 – 30% | 71 | Transition Ramp Down Long Smooth 2 – 100 to 0% | 112 | Transition Ramp Up Long Sharp 1 – 0 to 50% |
| 31 | Short Double Click Medium 1 – 100% | 72 | Transition Ramp Down Medium Smooth 1 – 100 to 0% | 113 | Transition Ramp Up Long Sharp 2 – 0 to 50% |
| 32 | Short Double Click Medium 2 – 80% | 73 | Transition Ramp Down Medium Smooth 2 – 100 to 0% | 114 | Transition Ramp Up Medium Sharp 1 – 0 to 50% |
| 33 | Short Double Click Medium 3 – 60% | 74 | Transition Ramp Down Short Smooth 1 – 100 to 0% | 115 | Transition Ramp Up Medium Sharp 2 – 0 to 50% |
| 34 | Short Double Sharp Tick 1 – 100% | 75 | Transition Ramp Down Short Smooth 2 – 100 to 0% | 116 | Transition Ramp Up Short Sharp 1 – 0 to 50% |
| 35 | Short Double Sharp Tick 2 – 80% | 76 | Transition Ramp Down Long Sharp 1 – 100 to 0% | 117 | Transition Ramp Up Short Sharp 2 – 0 to 50% |
| 36 | Short Double Sharp Tick 3 – 60% | 77 | Transition Ramp Down Long Sharp 2 – 100 to 0% | 118 | Long buzz for programmatic stopping – 100% |
| 37 | Long Double Sharp Click Strong 1 – 100% | 78 | Transition Ramp Down Medium Sharp 1 – 100 to 0% | 119 | Smooth Hum 1 (No kick or brake pulse) – 50% |
| 38 | Long Double Sharp Click Strong 2 – 80% | 79 | Transition Ramp Down Medium Sharp 2 – 100 to 0% | 120 | Smooth Hum 2 (No kick or brake pulse) – 40% |
| 39 | Long Double Sharp Click Strong 3 – 60% | 80 | Transition Ramp Down Short Sharp 1 – 100 to 0% | 121 | Smooth Hum 3 (No kick or brake pulse) – 30% |
| 40 | Long Double Sharp Click Strong 4 – 30% | 81 | Transition Ramp Down Short Sharp 2 – 100 to 0% | 122 | Smooth Hum 4 (No kick or brake pulse) – 20% |
| 41 | Long Double Sharp Click Medium 1 – 100% | 82 | Transition Ramp Up Long Smooth 1 – 0 to 100% | 123 | Smooth Hum 5 (No kick or brake pulse) – 10% |

## PCB LAYOUT RECOMMENDATIONS

In making the pad size for the WCSP balls, it is recommended that the layout use nonsolder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 24 and Table 2 show the appropriate diameters for a WCSP layout. The TPA2010D1 evaluation module (EVM) layout is shown in the next section as a layout example.

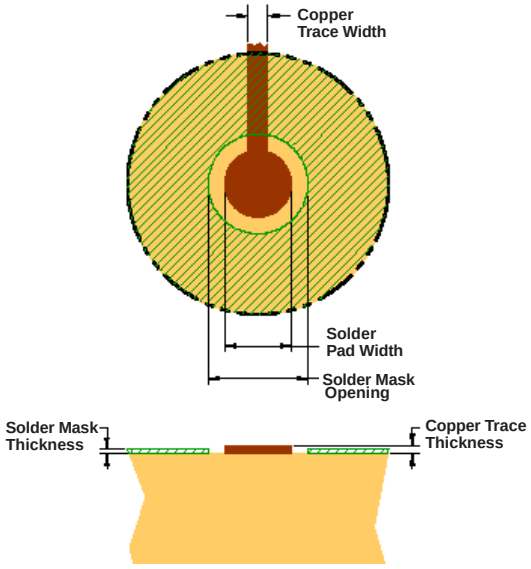



**Figure 24. Land Pattern Dimensions**

**Table 2. Land Pattern Dimensions**

| SOLDER PAD DEFINITIONS | COPPER PAD | SOLDER MASK OPENING | COPPER THICKNESS | STENCIL OPENING | STENCIL THICKNESS |
|---|---|---|---|---|---|
| Nonsolder mask defined (NSMD) | 275 µm (+0.0, –25 µm) | 375 µm (+0.0, –25 µm) | 1 oz max (32 µm) | 275 µm x 275 µm Sq. (rounded corners) | 125 µm thick |

**NOTES:**

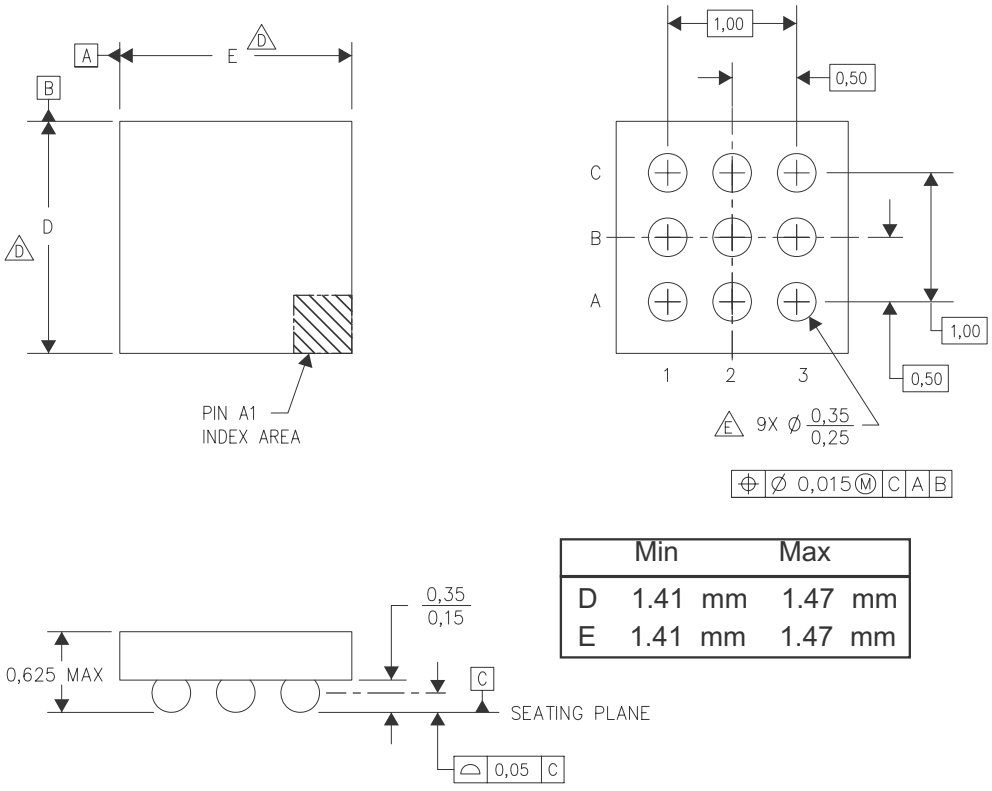
1. Circuit traces from NSMD defined PWB lands should be 75 µm to 100 µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
2. Recommend solder paste is Type 3 or Type 4.
3. Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
4. For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 µm to avoid a reduction in thermal fatigue performance.
5. Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
6. Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
7. Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

### Trace Width

Recommended trace width at the solder balls is 75 µm to 100 µm to prevent solder wicking onto wider PCB traces. Maintain this trace width until the ball pattern is escaped, then the trace width may be increased for improved current flow. The width/length of the 75 µm to 100 µm traces should be as symmetrical as possible around the device to give even solder reflow on each of the balls.

## MECHANICAL DATA

YZF (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY




| | Min | Max |
|---|---|---|
| D | 1.41 mm | 1.47 mm |
| E | 1.41 mm | 1.47 mm |

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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population. 3 x 3 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls. Refer to YEF (Drawing #4204181) for tin–lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.

# REVISION HISTORY

**Changes from Revision A (March 2013) to Revision B** **Page**

- Changed from 1 page data sheet to full data sheet in product folder ..... 1

**Changes from Original (December 2012) to Revision A** **Page**

- Changed $|I_{IH}|$ MAX value from 3 to 3.5µA per CMS #C1303020 ..... 4

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV2605YZFR | ACTIVE | DSBGA | YZF | 9 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 2605 | Samples |
| DRV2605YZFT | ACTIVE | DSBGA | YZF | 9 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 2605 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

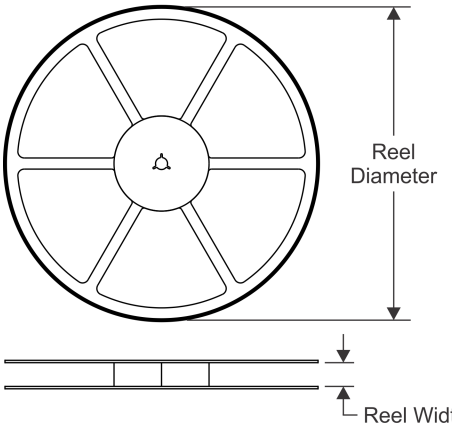
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

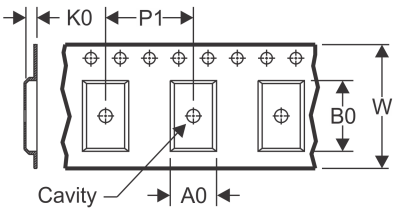
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

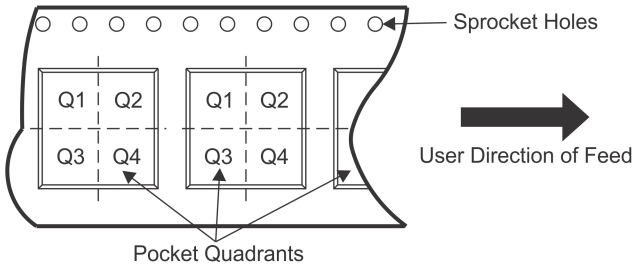



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

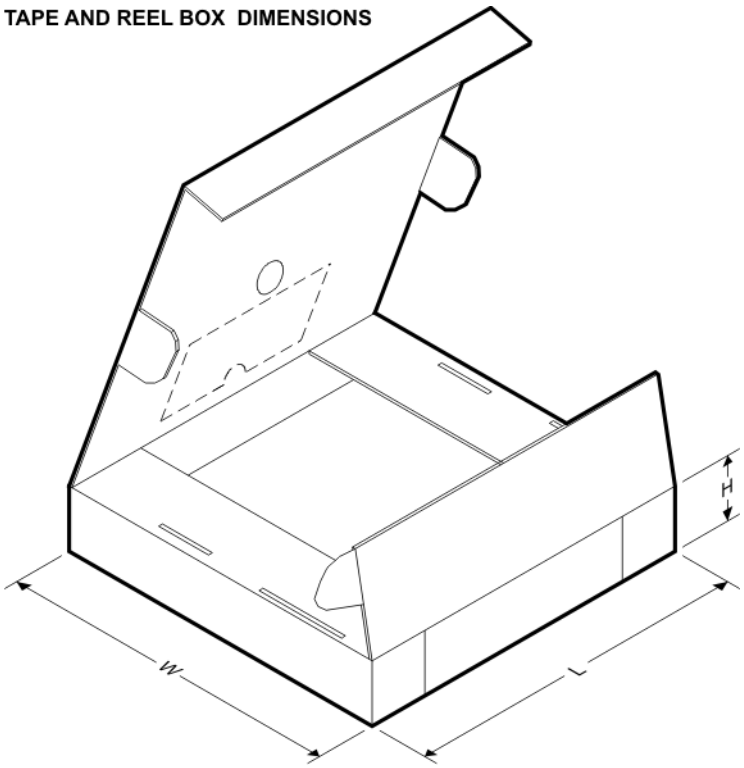
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV2605YZFR | DSBGA | YZF | 9 | 3000 | 180.0 | 8.4 | 1.65 | 1.65 | 0.81 | 4.0 | 8.0 | Q1 |
| DRV2605YZFR | DSBGA | YZF | 9 | 3000 | 178.0 | 9.2 | 1.65 | 1.65 | 0.81 | 4.0 | 8.0 | Q1 |
| DRV2605YZFT | DSBGA | YZF | 9 | 250 | 178.0 | 9.2 | 1.65 | 1.65 | 0.81 | 4.0 | 8.0 | Q1 |
| DRV2605YZFT | DSBGA | YZF | 9 | 250 | 180.0 | 8.4 | 1.65 | 1.65 | 0.81 | 4.0 | 8.0 | Q1 |

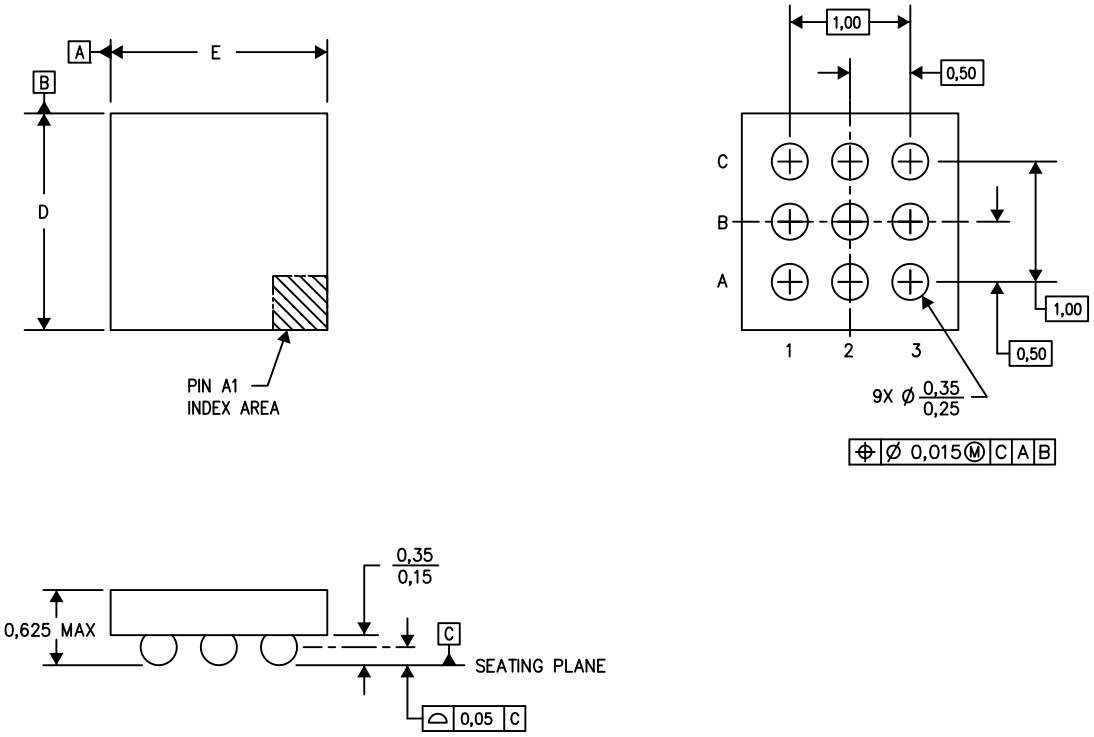
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV2605YZFR | DSBGA | YZF | 9 | 3000 | 182.0 | 182.0 | 17.0 |
| DRV2605YZFR | DSBGA | YZF | 9 | 3000 | 270.0 | 225.0 | 227.0 |
| DRV2605YZFT | DSBGA | YZF | 9 | 250 | 270.0 | 225.0 | 227.0 |
| DRV2605YZFT | DSBGA | YZF | 9 | 250 | 182.0 | 182.0 | 17.0 |

YZF (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY




D: Max = 1.47 mm, Min = 1.41 mm

E: Max = 1.47 mm, Min = 1.41 mm

4205058–4/P 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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