6A Buck Regulator with Integrated Inductor and Digital Power System Management

Features

- Package with output inductor included
- Small size: 3.3mm x 3.3mm x 1.485mm
- Continuous 6A load capability for AKM2800A
- Continuous 4A load capability for AKM2800B
- No external compensation required
- Programmable operation using the I²C serial bus
- Wide input voltage range: 4.5V–16V
- AKM2800A: output voltage 0.6V–2.6V
- AKM2800B: output voltage 3.3V and 5.0V
- Enabled input, programmable under-voltage lock-out (UVLO)
- Open-drain power-good indicator
- Built-in protection features
- Input voltage, output voltage, and junction temperature reporting
- Lead-free and halogen-free

Applications

- Storage applications
- Telecom and networking applications
- Industrial applications
- Server applications
- Distributed point-of-load power architectures
- Computing peripheral voltage regulation
- General DC-DC conversion

General Description

The AKM2800 is an easy-to-use, fully integrated, and highly efficient voltage regulator with voltage and temperature reporting. The on-chip pulse-width modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment. The ability to program aspects of the operation using the Inter-Integrated circuit (I²C) protocol is unique in this class of product. Developing and optimizing all these elements together has yielded the smallest, most efficient, and fully featured 6A currently available. The built-in protection features include pre-biased start-up, soft-start function, over-voltage protection, over-current protection with current clamp mode, thermal shut-down with auto-recovery. Furthermore, the AKM2800 provides accurate analog-to-digital converter for output voltage and junction temperature measurement to report the regulator parameters. The host can monitor the information by I²C serial interface.

Typical Applications

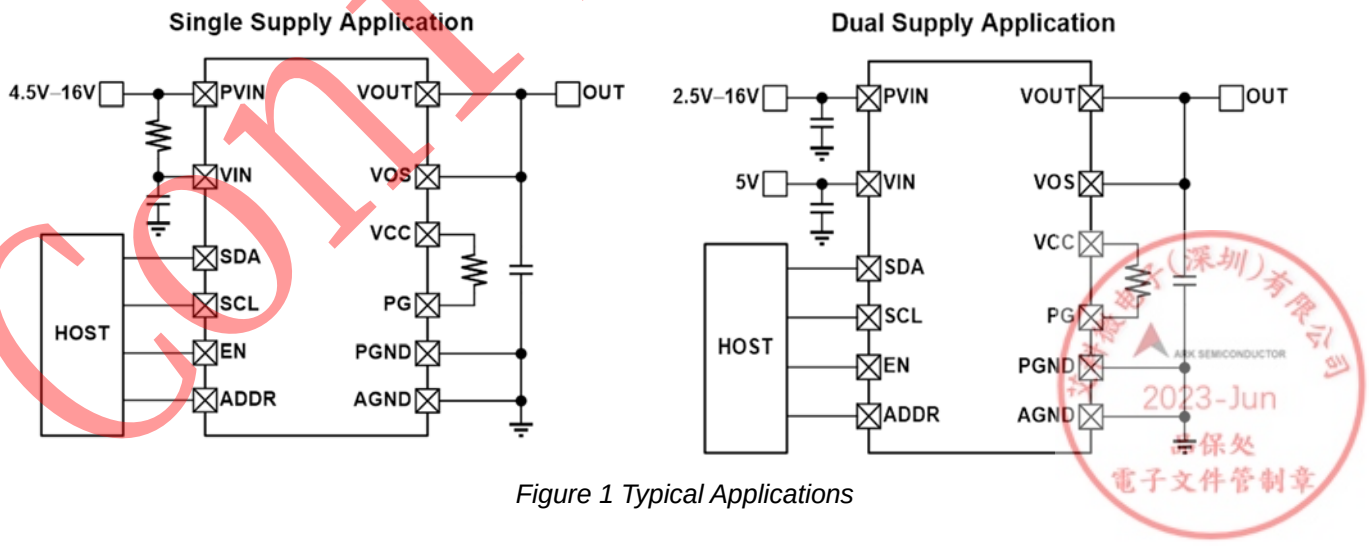


Figure 1 Typical Applications

Pin Configurations

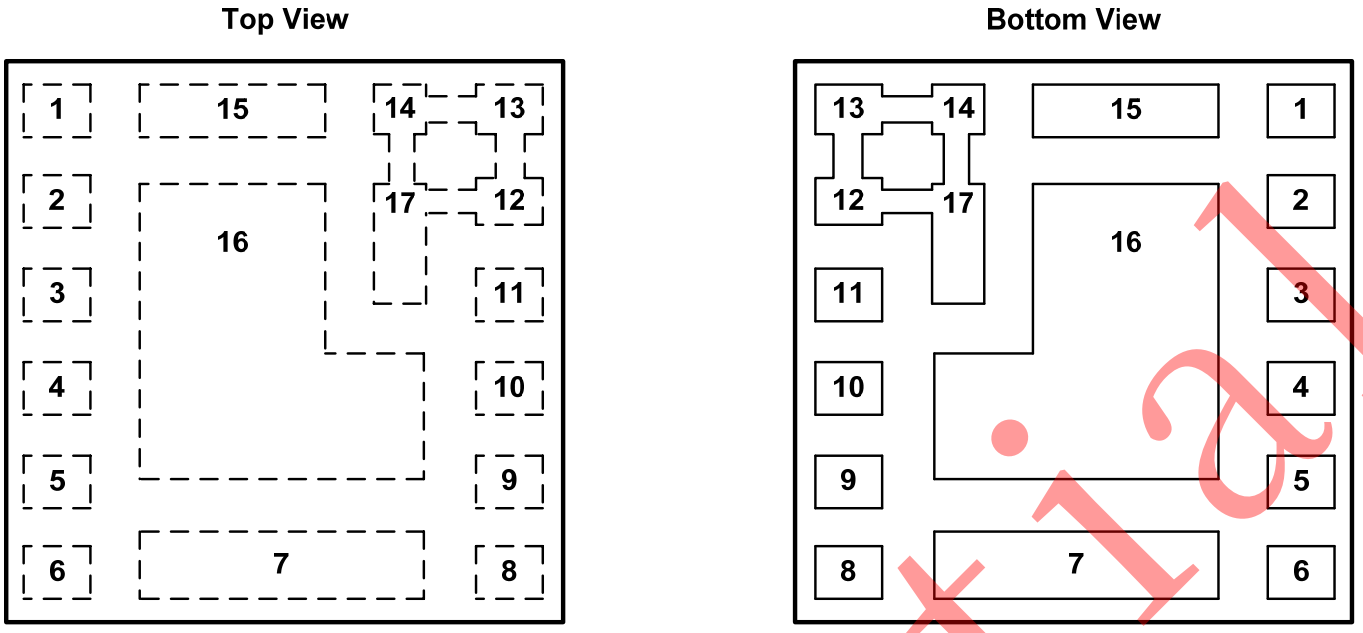


Figure 2 Pin layout

Functional Pin Description

Pin Number	Pin Name	Pin Function
1	SDA	I2C data serial input/output pin. Pull up to bus voltage with a 4.99kΩ resistor.
2	PG	Power good status pin. Open drain of an internal MOSFET. Pull up to VCC pin or an external bias voltage with a 49.9kΩ resistor.
3	EN	Enable pin. Switches IC on/off. Can be used with two external resistors to set an external UVLO.
4	SCL	I2C Clock pin. Pull up to bus voltage with a 4.99kΩ resistor.
5	VOS	VOUT sense pin. Connect directly to the regulator output.
6	ADDR	Address sense pin. Connect to AGND through a resistor to program IC address.
7	VOUT	Regulator output voltage pin. Place output capacitors between this pin and PGND.
8,16	PGND	Power ground pin. Serves as a separate ground for the MOSFETs. Connect to the power ground plane in the application.
9	AGND	Signal ground pin. Serves as the ground for the internal reference and control circuitry.
10	VCC	Supply voltage pin. May be an input bias for an external voltage or the output of the internal LDO regulator.
11	VIN	Input voltage pin. Input for the internal LDO regulator.
12, 13, 14, 17	PVIN	Power input voltage pin. Input for the MOSFETs.
15	VSW	Test point for internal VSW. Connect to an isolated pad on the PCB.

Order Information

Base Part Numbers	Package	Output Voltage	Part Numbers	Product Code	Shipping Method
AKM2800A	LGA3.3X3.3	0.60V	AKM2800A06POL	1	3000 （Tape & reel）
		0.70V	AKM2800A07POL	8	
		0.75V	AKM2800A7EPOL	9	
		0.80V	AKM2800A08POL	A	
		1.00V	AKM2800A10POL	2	
		1.05V	AKM2800A1EPOL	B	
		1.10V	AKM2800A11POL	C	
		1.20V	AKM2800A12POL	3	
		1.80V	AKM2800A18POL	5	
		2.50V	AKM2800A25POL	D	
AKM2800B		3.30V	AKM2800B33POL	6	
		5.00V	AKM2800B50POL	7	

TOP MARKING (AKM2800A/B)

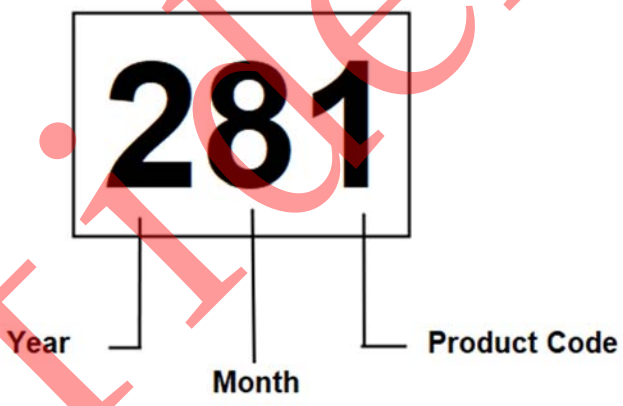


Figure 3 AKM2800A/B Marking

Y: Year code

M: Month Code

D: Product Code

Functional Block Diagram

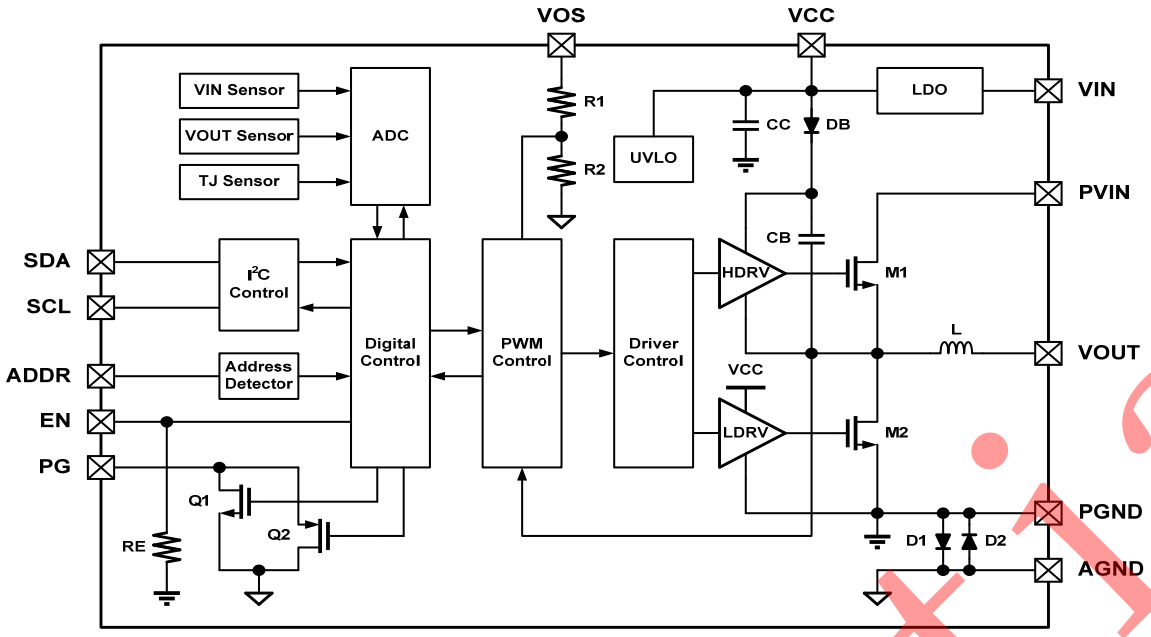


Figure 4 AKM2800 Block Diagram

Absolute Maximum Ratings

- Supply Pin Voltage, PVIN, VIN ---------- –0.3V to 18V
- SW to PGND ---------- –0.3V to 18V
- SW to PGND (25ns) ---------- –2.0V to 25V
- Control Pin Voltage, EN ---------- –0.3V to 18V
- Terminal Pin Voltage, VCC ---------- –0.3V to 6V
- Sense Pin Voltage, VOS ---------- –0.3V to 6V
- Terminal Pin Voltage, PG ---------- –0.3V to 6V
- Communication Pin Voltage, SCL SDA ---------- –0.3V to 6V
- Ground Pin Voltage, AGND to PGND ---------- –0.3V to +0.3V
- Junction Temperature Range ---------- –40°C to 150°C
- Storage Temperature Range ---------- –55°C to 150°C
- Junction to Ambient Thermal Resistance, θ_{JA} ---------- 26.5°C/W
- ESD Voltage Protection, Human Body Model ---------- 2KV

Recommended Operating Conditions

- Input Voltage Range with External VCC ---------- 2.5V to 16V
- Input Voltage Range with Internal LDO(AKM2800A) ---------- 4.5V to 16V
- Input Voltage Range with Internal LDO(AKM2800B) ---------- 8.0V to 16V
- Output Voltage Range (AKM2800A ---------- 0.6V to 2.6V
- Output Voltage Range (AKM2800B) ---------- 3.3V to 5.0V
- Continuous Output Current Range (AKM2800A) ---------- 0A to 6A
- Continuous Output Current Range (AKM2800B) ---------- 0A to 4A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(TA = 25°C, 0°C<TJ<125°C, 4.5V<PVIN=VIN<16V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VIN Supply Current Standby	$I_{IN\_STANDBY}$	EN=0V	--	1	2	mA
VIN Supply Current Static	I_{IN_STATIC}	EN=2V, No switching	--	2	3	mA
VIN Supply Current Dynamic	$I_{IN\_DYNAMIC}$	EN>2V, VIN=12V, VOS=1.8V, FSW=2MHz (AKC2800A)	--	19	25	mA
		EN>2V, VIN=12V, VOS=5.0V, FSW=1.4MHz (AKC2800B)	--	19	25	mA
Soft-Start						
Soft-Start Rate	t_{SS_RATE}	AKM2800A (Note 2)	--	0.5	--	V/ms
		AKM2800B (Note 2)	--	1.0	--	
Output Voltage						
Output Voltage Resolution	V_{OS_RES}	VOS≤1.8V	--	5	--	mV
		VOS>1.8V	--	10	--	mV
Output Voltage Accuracy	V_{OS_ACC}	PVIN=12V, VOS=1.8V, T_J=25°C	-0.5	--	+0.5	%
		PVIN=12V, 0.6V<VOS<1.0V, 25°C <T_J<125°C (Note 1)	-1.2	--	+1.2	%
		PVIN=12V, 1.0V<VOS<2.5V, 25°C <T_J<125°C (Note 1)	-1	--	+1	%
		PVIN=12V, 3.3V, 25°C <T_J<125°C(Note 1)	-1	--	+1	%
		PVIN=12V, 5.0V, 25°C <T_J<125°C (Note 1)	-1.2	--	+1.2	%
On-Time Timer Control						
On Time	t_{ON}	PVIN=12V, VOS=1.8V, FSW=2.0MHz (AKM2800A)	-	80	-	ns
		PVIN=12V, VOS=5.0V, FSW=1.4MHz (AKM2800B)	-	305	-	ns
Minimum On-Time	t_{ON_MIN}	(Note 2)	--	50	--	ns
Minimum Off-Time	t_{OFF_MIN}	(Note 2)	--	220	256	ns
Internal Low Drop-Out Regulator (LDO)						
LDO Output Voltage Accuracy	V_{CC_ACC}	5.5V<VIN≤16V, 0–20mA (Note 2)	4.9	5.2	5.5	V
		4.5V≤VIN<5.5V, 0–20mA (Note 2)	4.3	--	--	V
Line Regulation	V_{CC_LINE}	5.5V<VIN≤16V, 20mA (Note 2)	--	--	50	mV
Load Regulation	V_{CC_LOAD}	0–20mA (Note 2)	--	--	100	mV
Short Circuit Current	I_{CC_SHORT}	(Note 2)	--	70	--	mA
VCC Under-Voltage Lock-Out (UVLO)						
VCC Rise Threshold	$V_{CC\_UVLO\_RISE}$	Voltage rising	3.8	4.0	4.2	V
VCC Fall Threshold	$V_{CC\_UVLO\_FALL}$	Voltage falling	3.6	3.8	4.0	V
EN Rise Threshold	V_{EN_RISE}	Voltage rising	1.1	1.2	1.3	V
EN Fall Threshold	V_{EN_FALL}	Voltage falling	0.9	1.0	1.06	V
EN Input Impedance	R_{EN_INPUT}	Internal Resistance	500	1000	1500	KΩ
Junction Over-Temperature Protection (TJ OTP)						
TJ OTP Default	$T_{J\_OTP\_DEF}$	Temperature rising(Note 2)	--	145	--	°C
TJ OTP Hysteresis	$T_{J\_OTP\_HYS}$	Temperature falling(Note 2)	--	25	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over-Current Protection (OCP)						
OCP Default (Avg.)	I_{OCP_DEF}	PVIN=12V, VOS=1.8V, T_J=25°C When PG Pull Low (AKM2800A)	7.1	7.8	8.5	A
		PVIN=12V, VOS=5.0V, T_J=25°C When PG Pull Low (AKM2800B)	4.7	5.6	6.5	
VOS Over-Voltage Protection (OVP)						
VOS OVP Default	$V_{OS\_OVP\_DEF}$	VOS rising to VOS=1.8V (Note 2)	115	120	125	VOS%
VOS OVP Hysteresis	$V_{OS\_OVP\_HYS}$	VOS falling from VOS=1.8V	--	5	--	VOS%
VOS OVP Delay	t_{OVP_DELAY}	(Note 2)	--	5	--	μs
VOS Power Good (PG)						
VOS PG Default	$V_{OS\_PG\_DEF}$	VOS rising to VOS=1.8V	85	90	95	VOS%
VOS PG Hysteresis	$V_{OS\_PG\_HYS}$	VOS falling from VOS=1.8V	--	5	--	VOS%
PG Sink Current	I_{PG_SINK}	PG=0.8V, EN=2V	--	9	--	mA
ADC Reporting						
ADC Data Rate	t_{ADC_RATE}	For each channel reporting	--	1	--	ms
PVIN ADC Range	$V_{PVIN\_ADC\_RAN}$	VCC>UVLO (Note 2)	0	--	16	V
PVIN ADC Accuracy	$V_{PVIN\_ADC\_ACC}$	VCC>UVLO (Note 2)	–125	--	125	mV
VOUT ADC Range	$V_{OUT\_ADC\_RAN}$	VCC>UVLO (AKM2800A) (Note 2)	0.3	--	2.85	V
	$V_{OUT\_ADC\_RAN}$	VCC>UVLO (AKM2800B) (Note 2)	0.6		5.7	V
VOUT ADC Accuracy	$V_{OUT\_ADC\_ACC}$	VCC>UVLO(AKM2800A) (Note 2)	–20	--	20	mV
	$V_{OUT\_ADC\_ACC}$	VCC>UVLO(AKM2800B) (Note 2)	–40	--	40	mV
TJ ADC Range	$T_{J\_ADC\_RAN}$	VCC>UVLO (Note 2)	–40	--	150	°C
TJ ADC Accuracy	$T_{J\_ADC\_ACC}$	VCC>UVLO (Note 2)	–5	--	5	°C
I²C Parameter (SDA, SCL)						
SDA, SCL High Level Input Threshold Voltage	V_{IH_I2C}	(Note 2)	1.5	--	--	V
SDA, SCL Low Level Input Threshold Voltage	V_{IL_I2C}	(Note 2)	--	--	0.4	V
SCL Clock Frequency	f_{CK_I2C}	(Note 2)	--	--	1000	KHz
I²C Address (ADDR)						
I²C Address offset	R_{ADDR_0K}	Base address+0	--	0	--	KΩ
	R_{ADDR_10K}	Base address+1	--	10	--	KΩ
	R_{ADDR_20K}	Base address+2	--	20	--	KΩ
	R_{ADDR_30K}	Base address+3	--	30	--	KΩ

Note 1: Hot and cold temperature performance is assured by correlation using statistical quality control, but not tested in production; performance at 25°C is tested and guaranteed in production environment.
Note 2: Guaranteed by design but not tested in production.

Efficiency characteristics

Conditions: TA = 25°C, unless otherwise specified. PVIN=VIN=12V

PVIN = 12V, Internal LDO used, IO = 0A-6A, and 0-3A room temperature, no air flow, all losses include CIN=22uF/25V x 2, COUT=22uF/6.3V x 3, BW=20MHz

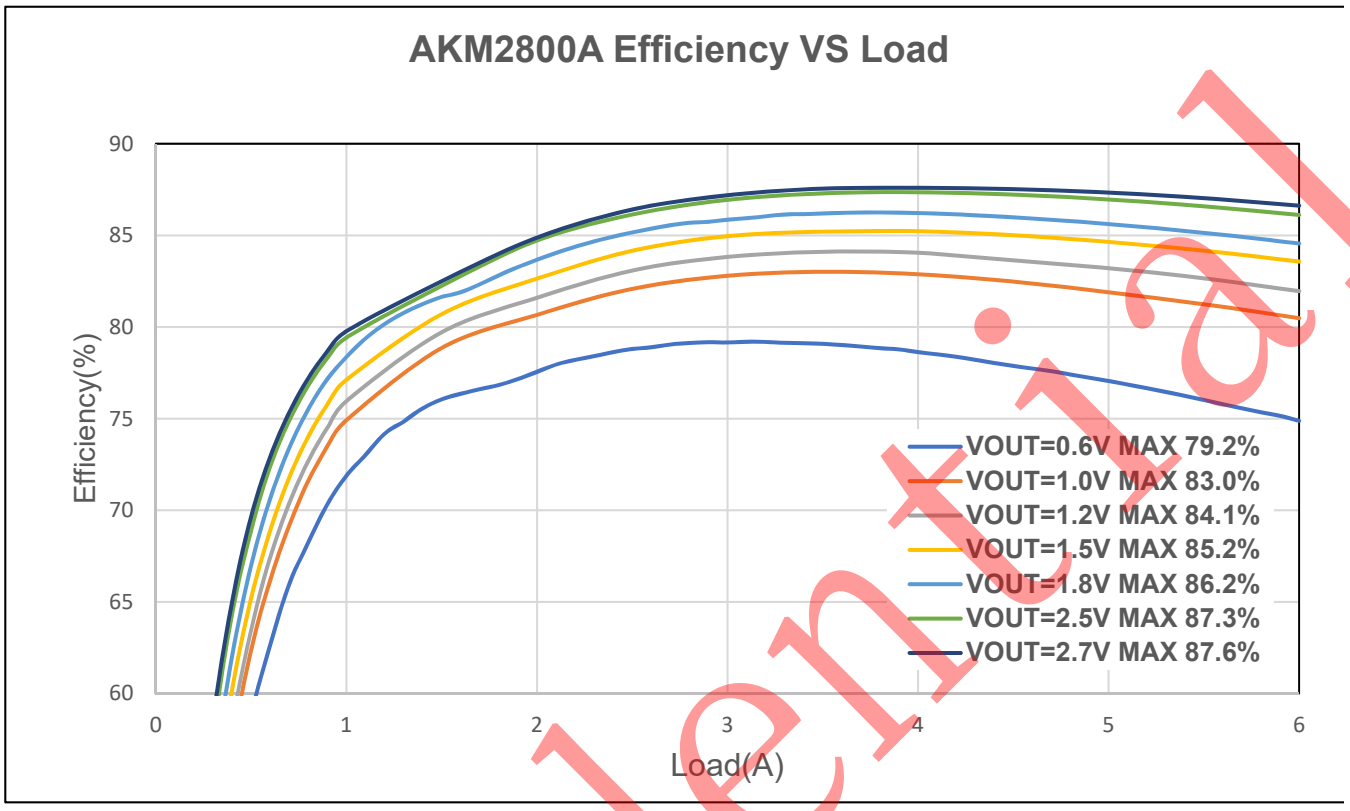


Figure 5 AKM2800A Efficiency VS Load

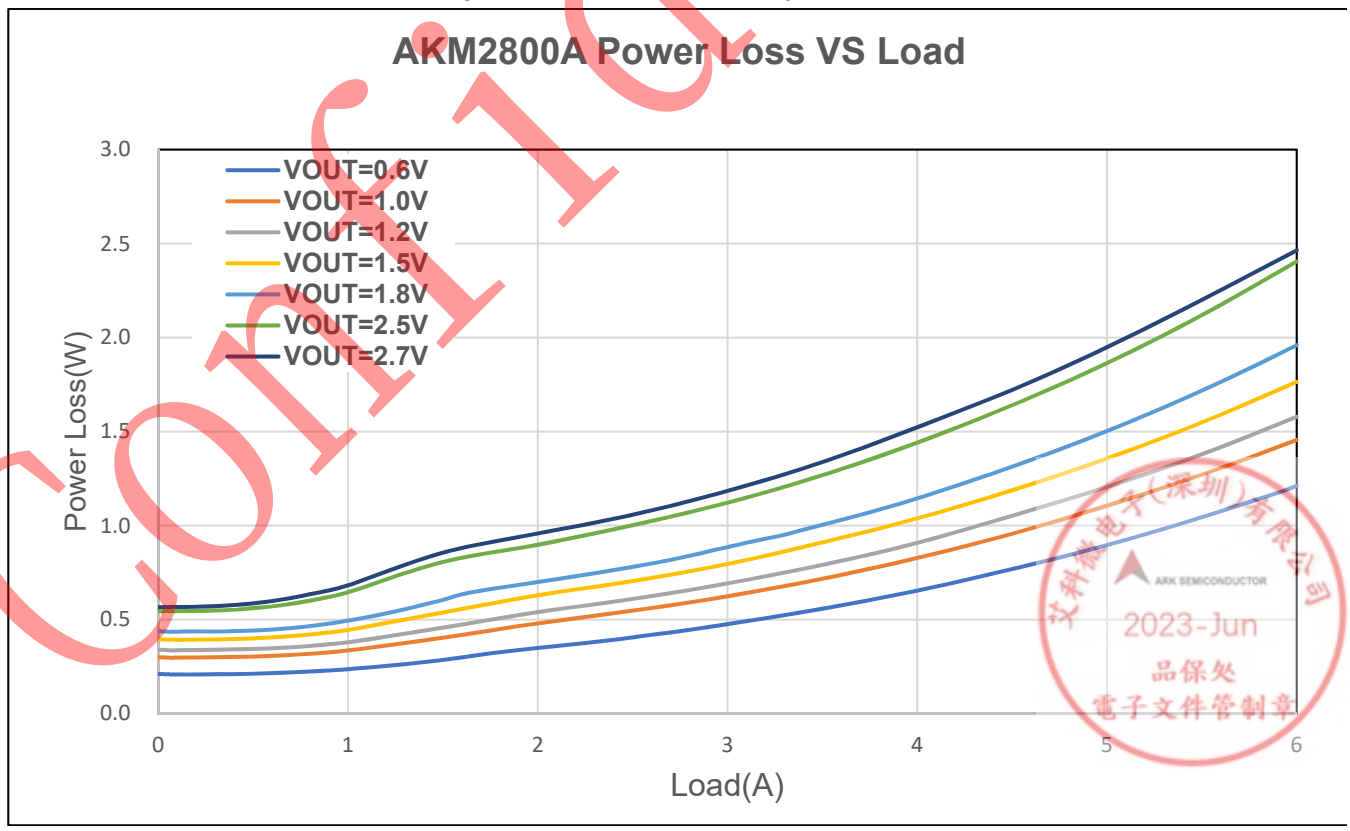


Figure 6 AKM2800A Power Loss VS Load

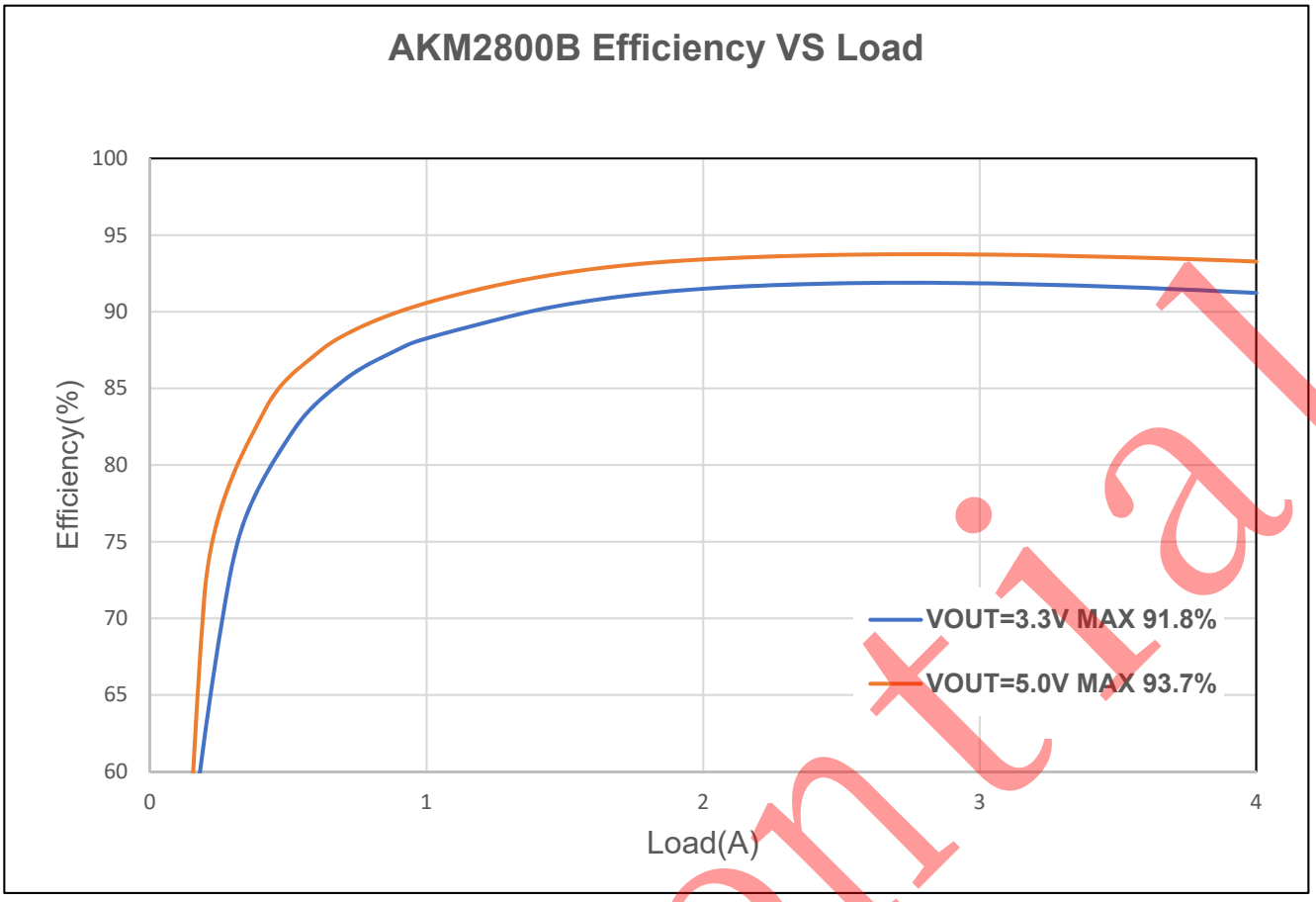


Figure 7 AKM2800B Efficiency VS Load

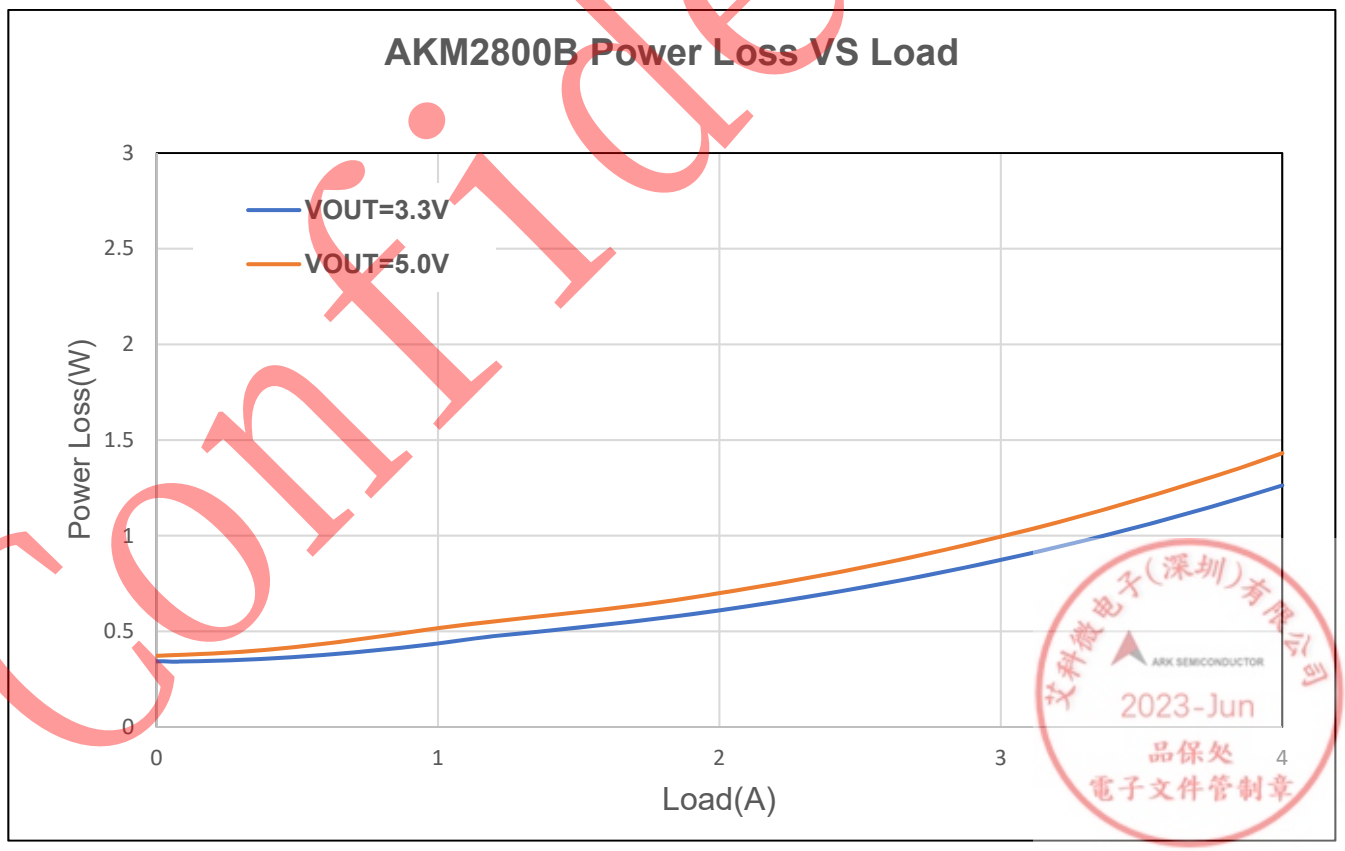


Figure 8 AKM2800B Power Loss VS Load

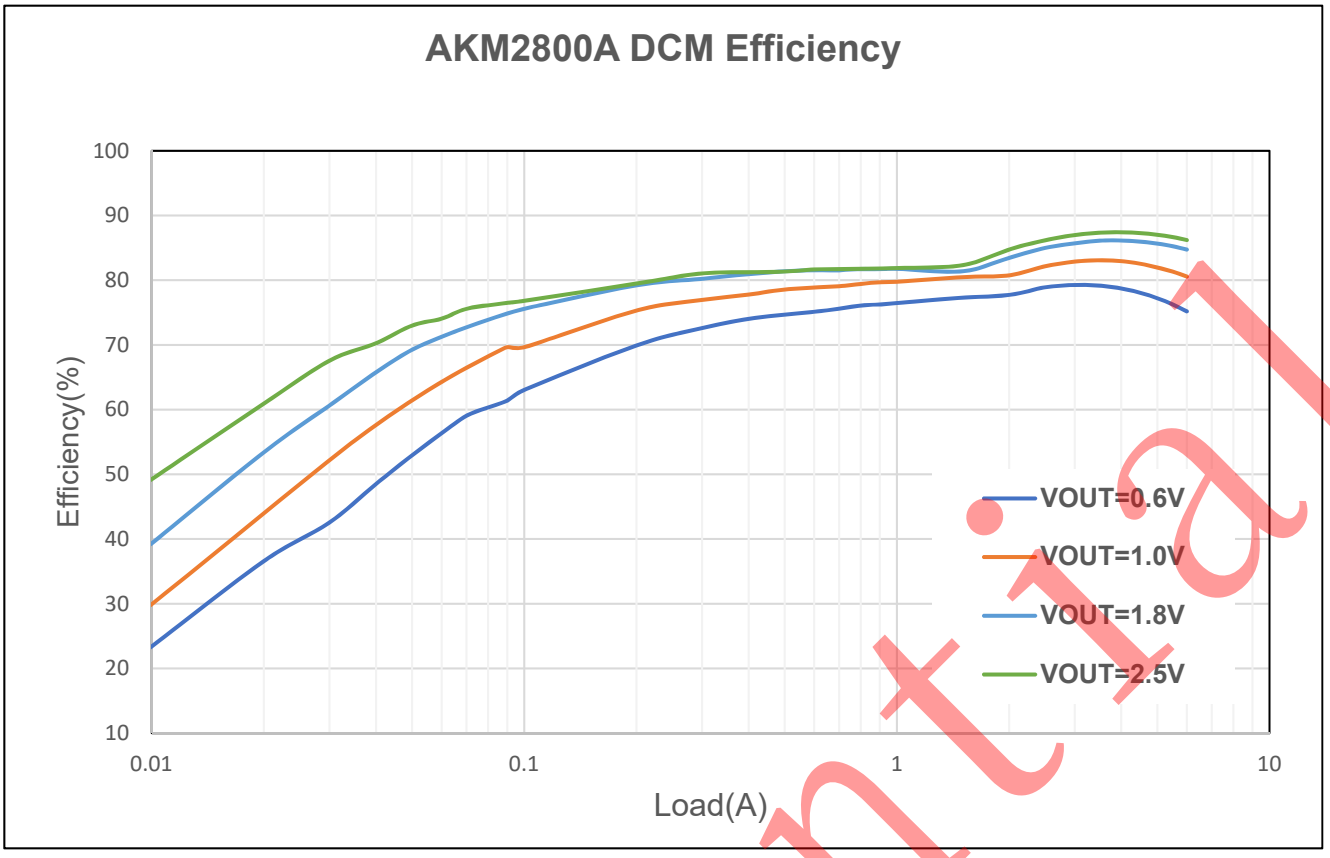


Figure 9 AKM2800A DCM Efficiency

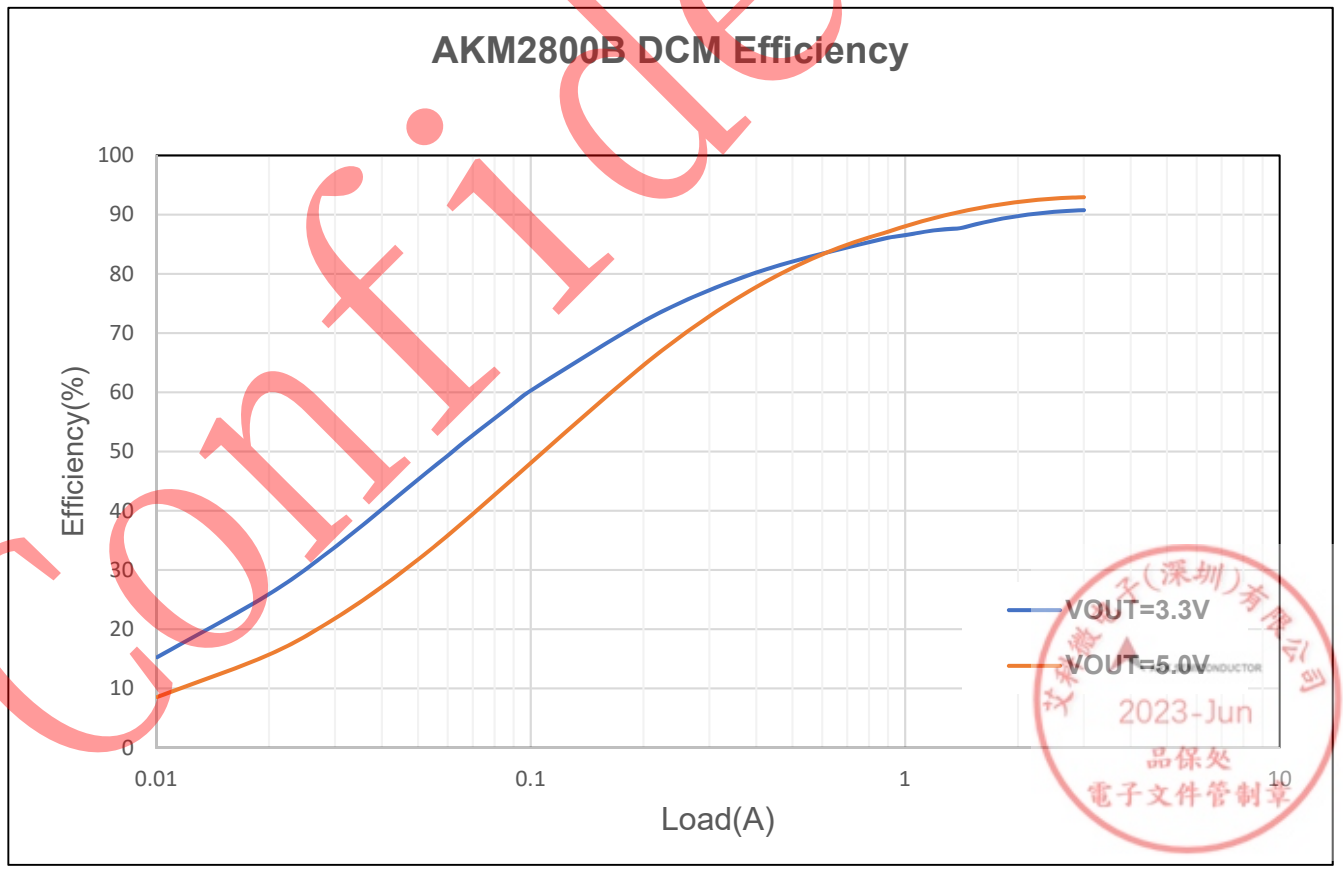


Figure 10 AKM2800B DCM Efficiency

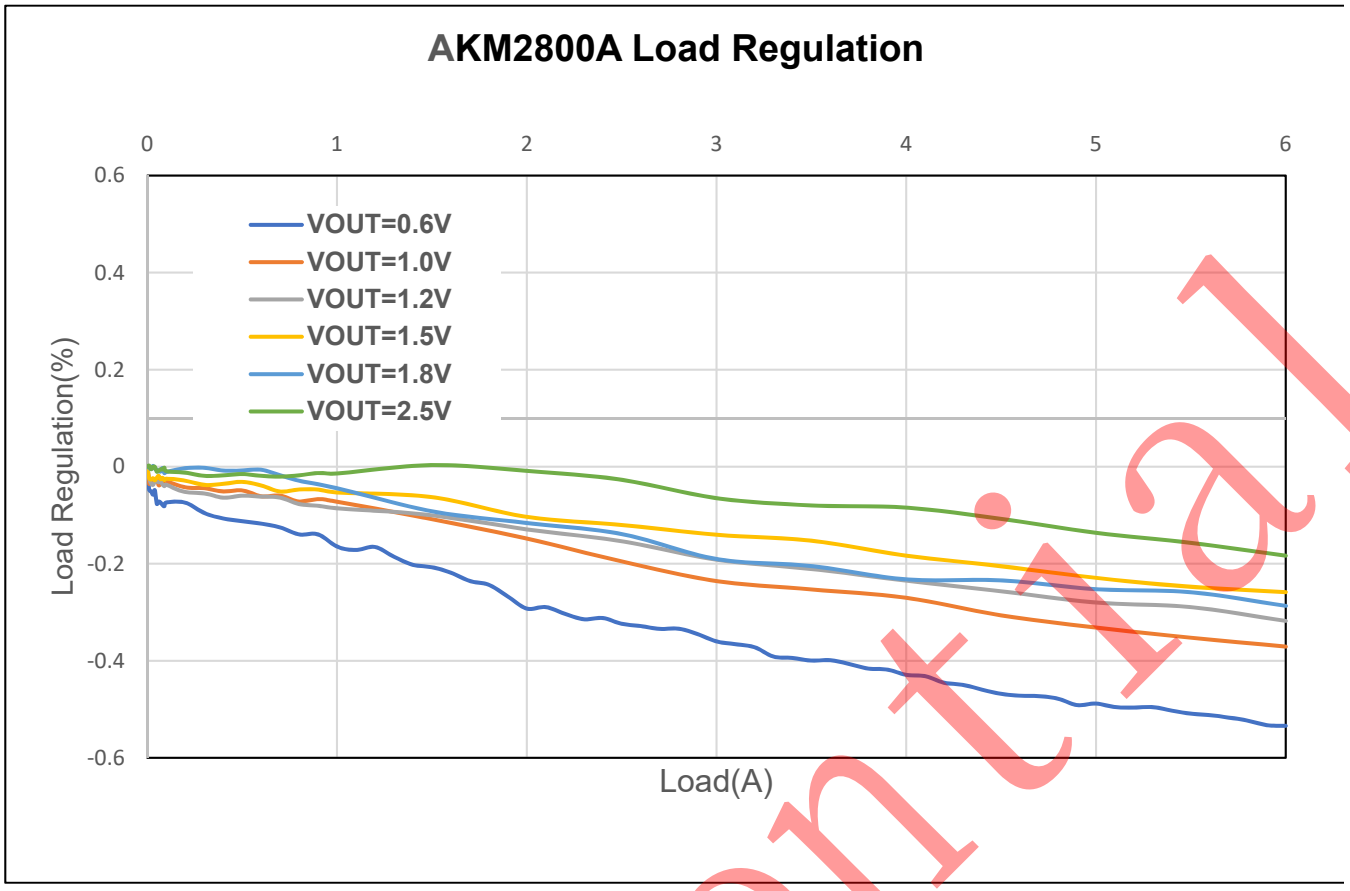


Figure 11 AKM2800A Load Regulation

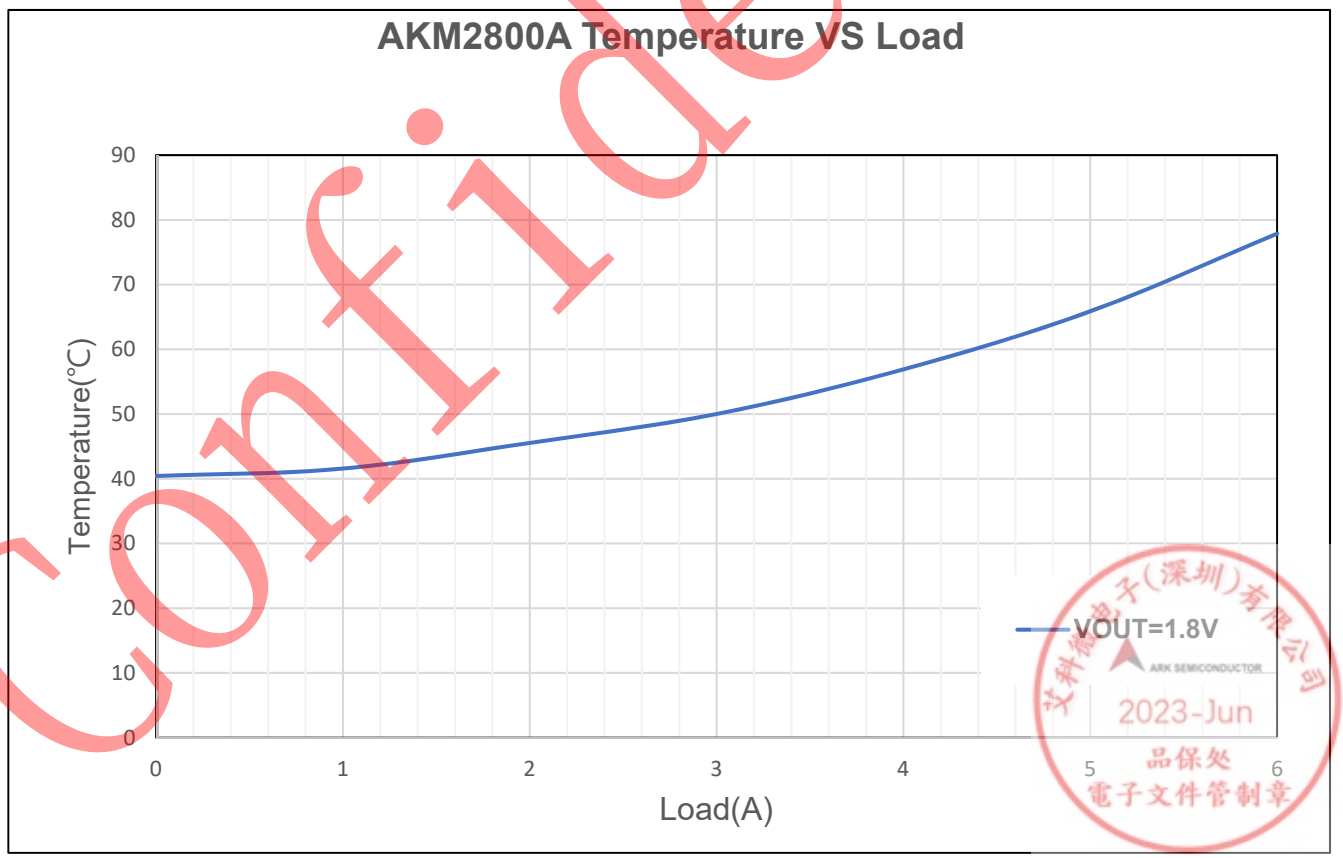


Figure 12 AKM2800A Temperature VS Load

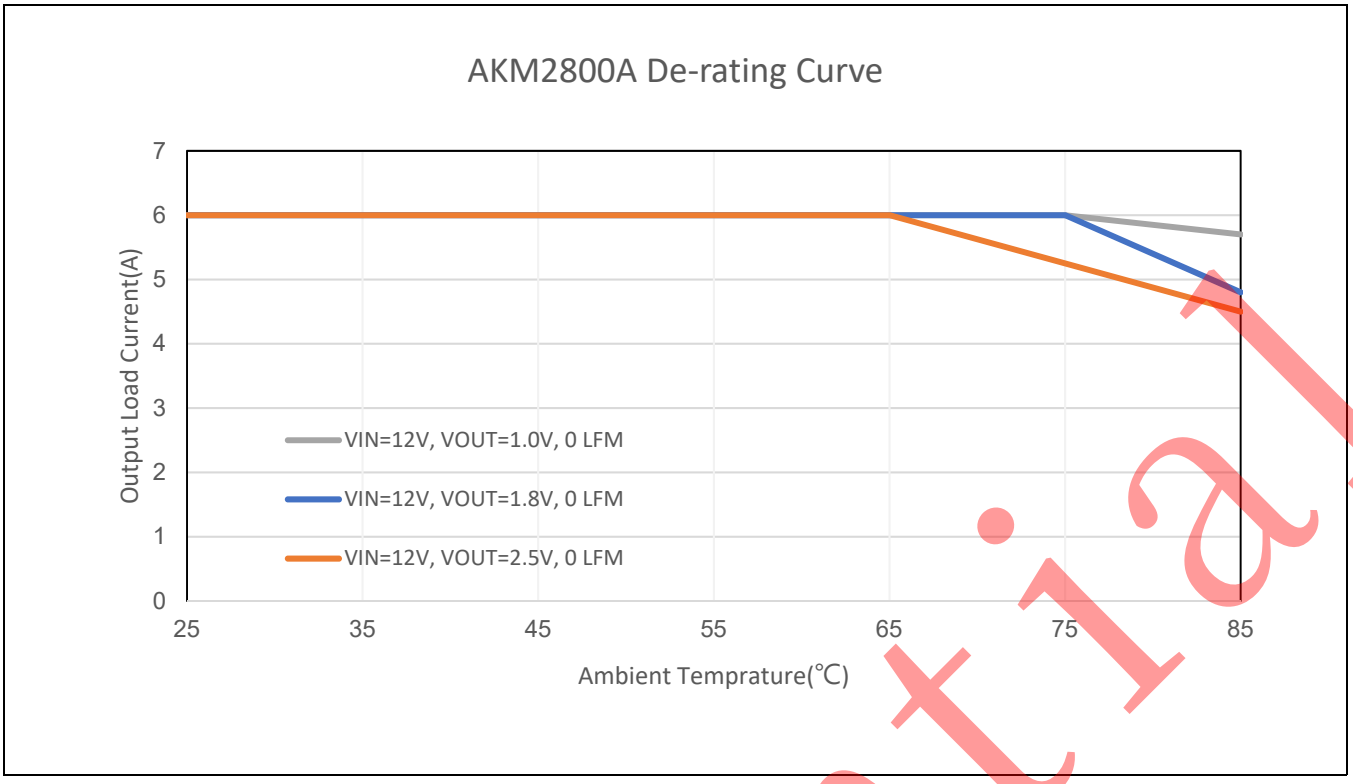


Figure 13 AKM2800A De-rating Curve

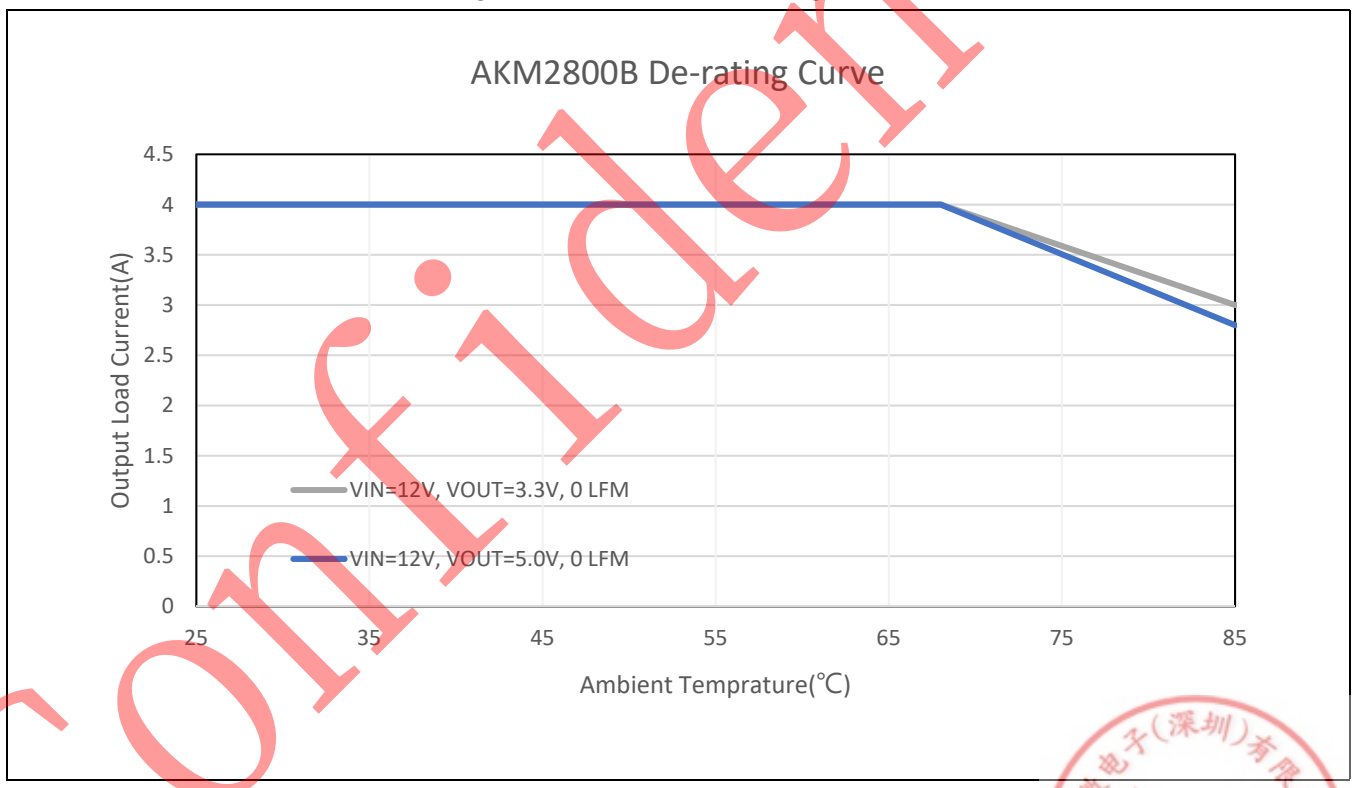


Figure 14 AKM2800B De-rating Curve

Typical Performance Characteristics: 1.8VOUT

Conditions: TA = 25°C, unless otherwise specified.

PVIN = 12V, Internal LDO used, IO = 0A-6A, room temperature, no air flow, all losses include

CIN=22uF/25V x 2, COUT=22uF/6.3V x 3, BW=20MHz

Figure 15 Power on for PVIN

CH1: VOUT CH2: VIN CH3: PG CH4: IOUT

Figure 16 Power off for PVIN

CH1: VOUT CH2: VIN CH3: PG CH4: IOUT

Figure 17 Power on for EN and Soft-Start

CH1: VOUT CH2: VIN CH3: PG CH4: IOUT

Figure 18 Power off for EN and Soft-off

CH1: VOUT CH2: VIN CH3: PG CH4: IOUT

Figure 19 VOUT Ripple and SW 0A

CH1: VOUT CH2: SW

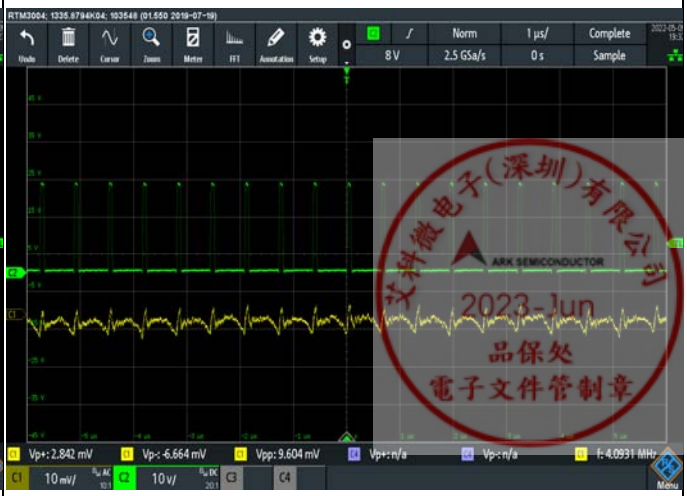


Figure 20 VOUT Ripple and SW 6A

CH1: VOUT CH2: SW

Figure 21 OCP for Clamp mode
CH1: VOUT CH2: SW CH3: PG CH4: IL

Figure 22 Clamp for REG_CYC_OCP [1:0] =2
CH1: VOUT CH2: SW CH3: PG CH4: IL

Figure 23 SCP for REG_CYC_OCP [1:0] =2
CH1: VOUT CH2: SW CH3: PG CH4: IL

Figure 24 OVP for DCM
CH1: VOUT CH2: VIN CH3: PG CH4: IOUT

Figure 25 Load Transient 10KHz
Load Range=0~4.2A Slew rate 7.5A/us
CH1: VOUT CH4: IOUT

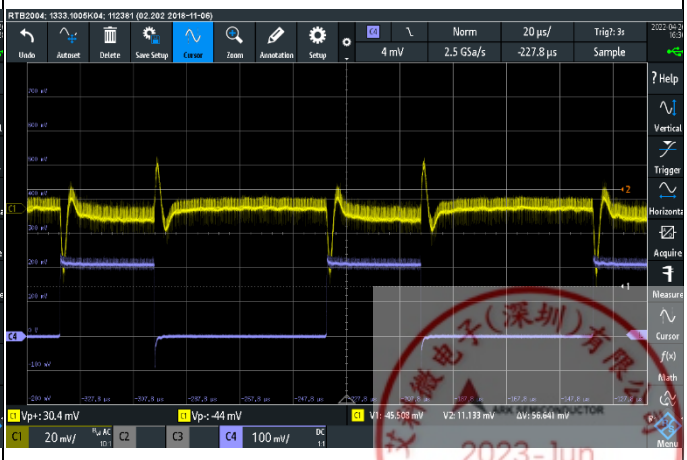


Figure 26 Load Transient 10KHz
Load Range=1.8~6A Slew rate 7.5A/us
CH1: VOUT CH4: IOUT

Applications information

Overview

The AKM2800 is an easy-to-use, fully integrated, and highly efficient DC/DC regulator. Aspects of its operation, including output voltage and system optimization parameters, can be programmed using the I2C protocol. It uses a proprietary modulator to deliver fast transient responses. The modulator has internal stability compensation so that it can be used in a wide range of applications, with various types of output capacitors, without loop stability issues.

Bias Voltage

The AKM2800 has an integrated Low Drop-Out (LDO) regulator, providing the DC bias voltage for the internal circuitry. The typical LDO regulator output voltage is 5.2V. For internally biased single-rail operation, the VIN pin must be connected to the PVIN pin (*Figure 27*). If an external bias voltage is used, the VIN pin must be connected to the VCC pin in order to bypass the internal LDO regulator (*Figure 28*). In either configuration, once the supply voltages are above the UVLO rise threshold, the device is enabled without EN pin. Consequently, the I2C communication begins as soon as:

- VCC_UVLO rise threshold is exceeded.
- Memory contents are loaded.
- Initialization is complete.
- Address offset is read.

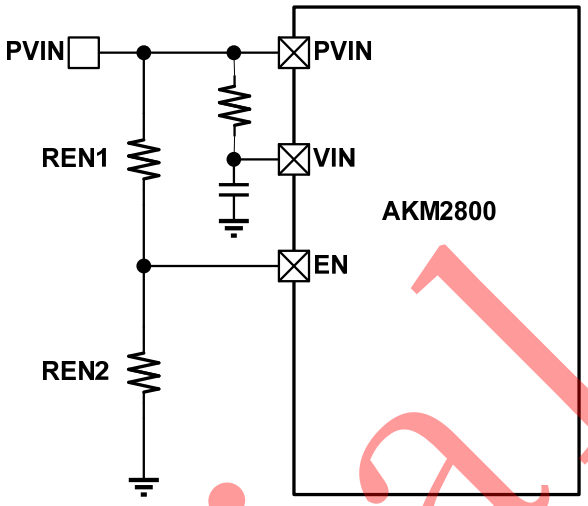


Figure 27. Single supply configuration: internal LDO regulator, adjustable PVIN UVLO

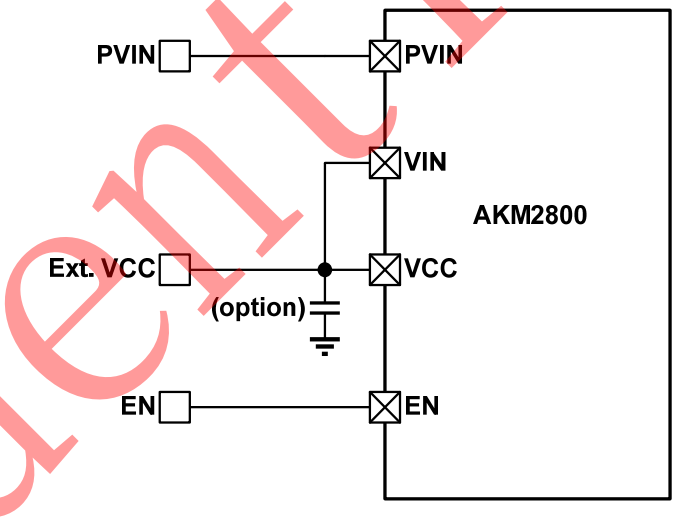


Figure 28 Using external bias voltage

I2C Base address and offsets

The AKM2800 has a user register called REG_BASE_ADDR<7:0> stored in memory that sets its base I2C address. The default base address is 0x08. An offset of 0-3 is then defined by connecting the ADDR pin to the AGND pin either directly or through a resistor. An address detector reads the resistance of the connection at startup and uses it to set the offset. This offset is then added to the base I2C address to set the address with which the I2C master device will communicate.

To select an offset of 0 to 3, connect the pins as follows:

- 0 – 0Ω (short ADDR to AGND)
- +1 – 10kΩ
- +2 – 20kΩ
- +3 – >30.1kΩ

Soft-start and target output voltage

The AKM2800A has an internal digital soft-start circuit to control output voltage rise-time and limit current surge at start-up. When VCC exceeds its start threshold (VCC_UVLO_RISE), the AKM2800 exits reset mode; this initiate loading of the contents of the non-volatile memory into the working registers and calculates the address offset as described above.

Once initialization is complete and the Enable pin is asserted (*Figure 29*), the internal reference soft starts to the target output voltage, then the power good with pull high. The output voltage soft start slew rate defined by the user register bit REG_SSTART_RATE.

REG_SSTART_RATE<4:3>		
Register	**Bit**	**Description**
0x14	<4:3>	Soft start rate 00: 0.5mV/us (default) 01: 1.0mV/us 10: 0.25mV/us 11: 2.0mV/us

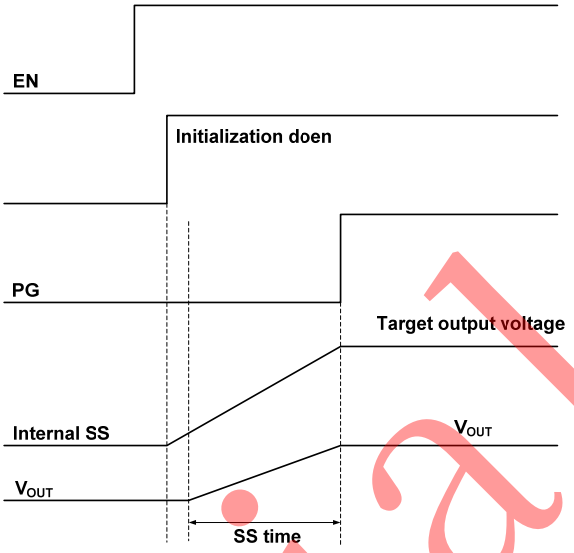


Figure 29. Operated waveforms during soft start

During initial start-up, the AKM2800A operates with a reduced-on time until the output voltage increases. On-time is increased until VOUT reaches the target value defined by the user register bit REG_VOS_REG<0> VOS Regulation MSB and user register REG_VOS_REG<7:0> VOS Regulation LSB.

REG_VOS_REG<0>, REG_VOS_REG<7:0>		
Register	**Bit**	**Description**
0x12	<0>	VOS Regulation MSB
0x13	<7:0>	VOS Regulation LSB

VOUT is set in increment of 5mV for target voltages from 0.6V to 2.6V. Using the following equation to calculate the V_{OUT} code to REG_VOS_REG<8:0>:

$$VOUT_{CODE}(DEC) = \frac{VOUT_{TARGET} - 0.4}{0.005}$$

For example1:

To set VOUT=1V:

$$VOUT_{CODE}(DEC) = \frac{1 - 0.4}{0.005} = 120$$

120 is 078 in hexadecimal, therefore: set VOS Regulation MSB to 0 and set VOS Regulation LSB to 78h.

For example2:

To set VOUT=2.5V:

$$VOUT_{CODE}(DEC) = \frac{2.5 - 0.4}{0.005} = 420$$

420 is 1A4 in hexadecimal, therefore: set VOS Regulation MSB to 1 and set VOS Regulation LSB to A4h.

Over-current protection (OCP) and over-voltage protection (OVP) are both enabled during soft start to protect the AKM2800A from short circuit and excess voltage, respectively.

For maximum system accuracy, the recommended method to set the output voltage is by programming the user registers with the appropriate code. For optimum performance when using this approach, the change in output voltage should not exceed ±20% of the pre-set default output voltage.

However, another option is to use AKM2800A default VOS voltage is 0.6V with a feedback resistor divider (*Figure 30*). This gives system designers the flexibility to design all the power rails in the system across the entire output voltage range (0.6V to 2.6V) using a single part, at the expense of a worst-case error of no more than an additional -1%.

If using a feedback resistor divider, the VOUT ADC reporting function max is 2.85V。

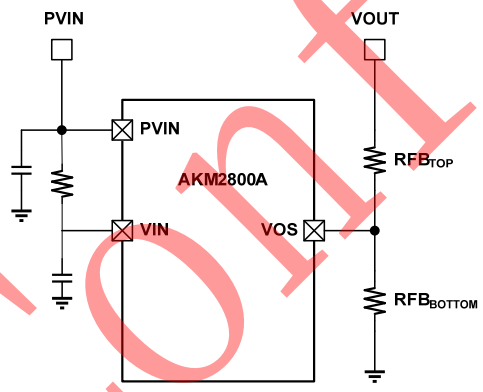


Figure 30. Setting output voltage with external resistor divider

The equation below describes the appropriate resistor divider selection to set the output voltage using AKM2800A programmed to 0.6V.

$$RFB_{BOTTOM} = \frac{222k * RFB_{TOP}}{370k * (VOUT - 0.6) - RFB_{TOP} * 0.6}$$

It is recommended that system designers to use 40K~50KΩ for RFB_{TOP}. The recommended value for RFB_{BOTTOM} depends on the output voltage by equation.

Pre-biased start-up

The AKM2800 can start up into a pre-charged output linearly when operating at DCM. When it starts up in this way, the high and low side MOSFETs are forced off until the internal Soft-Start (SS) voltage exceeds the sensed output voltage at the VOS pin. Only then is the first gate signal of the high side MOSFET generated, followed by the turn on of the low side MOSFET. The Power Good (PG) function is not active at this point.

Shut-down Mechanisms

The AKM2800 shut-down mechanisms:

- The hardware shutdown is initiated by de-asserting the EN pin. When EN signal from high to low level, the power good reaches low level immediately, then the output voltage always follows the SS signal down to 0V.
- Software shutdown controlled is initiated by setting user register bit REG_SW_SSTOP_EN to 1 and user register bit REG_SW_SSTOP_CTL to 0.

The REG_SW_SSTOP_EN and REG_SW_SSTOP_CTL cat of during start-up; the drivers are disabled only when the output voltage reaches 0. The output voltage then follows the SS signal down to 0V.

The REG_SW_SSTOP_EN bit must not be toggled while the part is switching. For applications requiring software stop, this bit must be set to 1. While the EN pin is asserted, the REG_SW_SSTOP_CTL bit must be used to start and off the device. By default, both bits are 0, which means that software operation is disabled by default.

REG_SW_SSTOP_EN, REG_SW_SSTOP_CTL		
Register	**Bit**	**Description**
0x14	<2>	Software enable
0x1C	<3>	Software control

REG_SW_SSTOP_CTL:	
Toggle	**Description**
0 → 1	Software turn-on
1 → 0	Software turn-off

Switching Frequency

The switching frequency of AKM2800A depends on the output voltage. For and output voltage of 1.8V, the switching frequency is nominally 1.95MHz.

When the output voltage is set by programming the user register or external resistor divider, the appropriate switching frequency is as below equation:

$F_{SW} = 650KHz * \frac{V_{OUT}}{0.6}$ for AKM2800A

$F_{SW} = 900KHz * \frac{V_{OUT}}{3.3}$ for AKM2800B

Therefore, with either method, system designers need not concern themselves with selecting the switching frequency and have one fewer design task to manage.

Enable (EN) pin

The Enable (EN) pin has several functions:

- The EN pin is used to turn the AKM2800 on and off. It has a precise threshold, which is internally monitored by the UVLO circuit. If the EN pin is left floating, an internal 1MΩ resistor pulls it down to prevent the device from being switched on unintentionally.
- The EN pin can also be used to implement a precise input voltage UVLO. The input of the EN pin is derived from the other rail voltage by a set of resistor dividers, REN1 and REN2 (*Figure 31*). Users can program the UVLO threshold voltage by selecting different ratios. When PVIN is lower than the desired voltage level, this can help to turn off the device.
- The EN pin can be directly connected to PVIN without external resistor dividers. This is a useful feature for single supply operation when there is no enable signal available to enable the device.
- The EN can be used to monitor other rails for a specific power sequencing scheme (*Figure 31*).

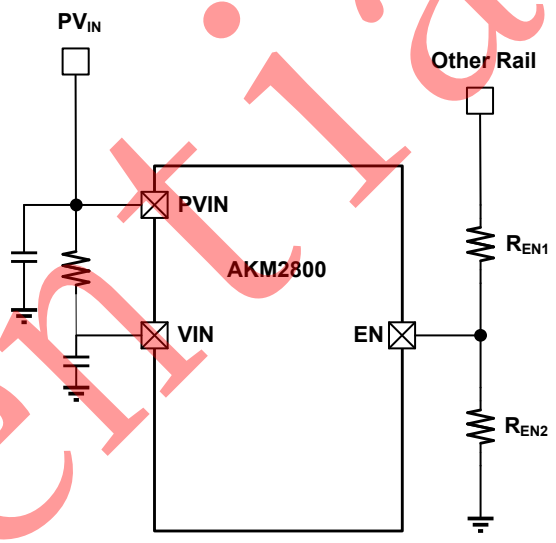


Figure 31. EN pin used to monitor other rails for sequencing purposes.

Over-current Protection (OCP)

Over-current protection (OCP) is provided by sensing the current through the $R_{DS(on)}$ of the low-side MOSFET. When this current exceeds the OCP threshold, a fault condition is generated. This method provides several benefits:

- Provides accurate overcurrent protection without reducing converter efficiency (the current sensing is lossless).
- Reduces overall system cost by eliminating a current sense resistor.
- Reduces any layout-related noise issue.

The threshold is internally temperature compensated so that it remains almost constant at different ambient

temperatures. When the current exceeds the OCP threshold, the PG and SS signals are pulled low.

The AKM2800 enters current clamp mode (*Figure 32*). Both high-side MOSFET and low-side MOSFET remain switching for the OCP threshold level. If an overcurrent fault is still detected, the preceding actions are repeated. The AKM2800 remains in current clamp mode until the over-current fault is removed.

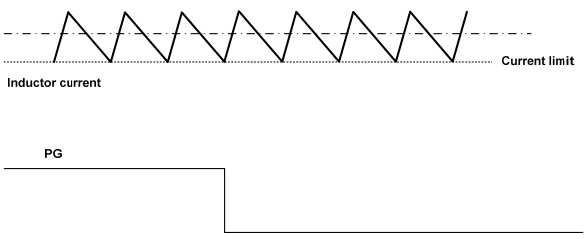


Figure 32. OCP clamp mode behavior

Over-voltage Protection (OVP)

Over-voltage protection (OVP) is provided by sensing the voltage at the VOS pin. When VOS exceeds the output OVP threshold for longer than the output OVP delay (typically 5μs), a fault condition is generated and PG pin is pulled low.

The OVP threshold is defined by the user Register bits REG_VOS_OVP<1:0>.

REG_VOS_OVP<1:0>		
Register	**Bit**	**Description**
0x17	<1:0>	VOS OVP 00: 105% of VOS 01: 110% of VOS 10: 115% of VOS 11: 120% of VOS (default)

If REG_VOS_OVP_RPS set to 1, it operated in OVP unlatched mode. When Vout is lower than OVP threshold with 5% hysteresis, PG re-asserts.

If REG_VOS_OVP_RPS set to 0, both MOSFETs remains latched off until reset by cycling either VCC or EN.

REG_VOS_OVP_RPS		
Register	**Bit**	**Description**
0x1A	<0>	VOS OVP Response 0: Latch (default) 1: Unlatch

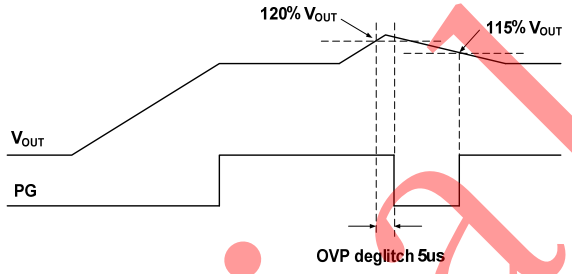


Figure 33. OVP unlatch mode behavior

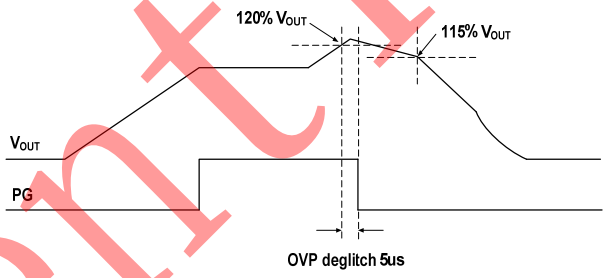


Figure 34. OVP latch-off mode behavior

Over-temperature Protection (OTP)

Temperature sensing is provided inside the AKM2800. The OTP threshold is defined by the User register bits REG_TJ_OTP<1:0>.

REG_TJ_OTP<1:0>		
Register	**Bit**	**Description**
0x19	<1:0>	TJ OTP 00: 75 Degree 01: 85 Degree 10: 125 Degree 11: 145 Degree (default)

When the threshold is exceeded, thermal shutdown switches off both high side and low side MOSFETs and resets the internal soft-start circuit, but the internal LDO regulator is still in operation.

In automatic restart mode, the sensed temperature

drops within the operating range. There is a 20°C hysteresis in the OTP threshold.

Power Good (PG)

Power Good (PG) behavior is defined by the User register bits REG_VOS_PG<1:0>.

REG_VOS_PG<1:0>		
Register	**Bit**	**Description**
0x18	<1:0>	VOS PG 00: 80% of VOS 01: 85% of VOS 10: 90% of VOS (default) 11: 95% of VOS

The user register bit REG_VOS_PG<1:0> defines the PG threshold as a percentage of VOUT. Hysteresis of 5% is applied to this, giving a lower threshold.

When VOS rises above the upper threshold, the PG signal is pulled high. When VOS drops below the lower threshold, the PG signal is pulled low.

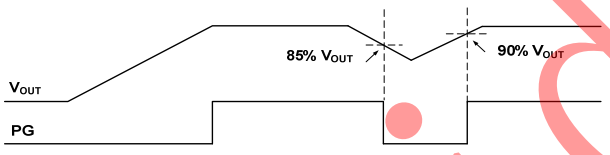


Figure 35 PG behavior

The PG signal is asserted when:

- EN and VCC are both above their threshold voltages
- No fault has occurred (OCP, OVP, OTP)
- VOUT is within the target range.

ADC telemetry reporting for PVIN, VOUT and Junction temperature

The AKM2800 has an internal ADC to monitor voltage of PVIN and VOUT pins and junction temperature. Reporting telemetry is defined by user register bits REG_PVIN_ADC<7:0>, REG_VOUT_ADC<7:0> and REG_TJ_ADC<7:0>.

REG_PVIN_ADC<7:0>		
Register	**Bit**	**Description**
0x0C	<7:0>	PVIN ADC Report LSB: 62.5mV Range: 0 to 15.9375V

REG_VOUT_ADC<7:0>		
Register	**Bit**	**Description**
0x0D	<7:0>	VOUT ADC Report LSB: 10mV Range: 0.3 to 2.85V

REG_TJ_ADC<7:0>		
Register	**Bit**	**Description**
0x0F	<7:0>	TJ ADC Report LSB: 1°C Range: -40°C to +150°C

Reporting data can be calculated as equation:

$PVIN$ = 0x0C(DEC) × $0.0625V$

$VOUT$ = 0x0D(DEC) × $0.01V + 0.3V$

TJ = 0x0F(DEC)-75 ℃

For example,

when read 0x0C=C0(hex), C0 is 192 in decimal, therefore:

$PVIN = 192 \times 0.0625V = 12V$

when read 0x0D=DC(hex), DC is 220 in decimal, therefore:

$VOUT = 220 \times 0.01V + 0.3V = 2.5V$

when read 0x0F=A0(hex), A0 is 160 in decimal, therefore:

$TJ = 160 - 75 = 85℃$

Input Capacitance

The input current to the step-down converter is discontinuous, and therefore, requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for best performance. During layout, place the input capacitors as close to PVIN pin as possible. The capacitance can vary significantly with temperature. Use capacitors with X5R and X7R ceramic dielectrics because they are fairly.

stable over a wide temperature range and they offer very low ESR. The capacitors must have a ripple current rating.

that exceeds the converter's maximum input ripple current. Estimate the input ripple current with equation:

$$I_{IN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{IN\_RMS} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current. MLCCs (multi-layer ceramic capacitors) are ideal. Typically, in 0805 size, they can handle 2A RMS current with less than 5°C temperature rise.

The input capacitor value determines the converter input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification. Estimate the input voltage ripple with equation:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times F_{SW}}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{I_{OUT}}{4 \times C_{IN} \times F_{SW}}$$

Output Capacitance

The output capacitor maintains the DC output voltage. Use MLCC capacitors and estimate the output voltage ripple with equation:

$$\Delta V_{OUT} = 4.55 \times \frac{V_{OUT} \times (1-D)}{F_{SW}} \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{SW}}\right) \times 10^9 \ mV$$

The design requires minimum output capacitance to meet the target peak-to-peak output voltage ripple.

where:

D = duty cycle

F_{SW} = switching frequency

R_{ESR} = equivalent series resistance of MLCC

ΔV_{OUT} = target peak-to-peak VOUT ripple

VCC Capacitance

The AKM2800 uses an on-package VCC capacitor to ensure effect high-frequency bypassing. However, especially for applications that use an external VCC supply, it is recommended that system designers place a 2.2uF/0603/X7R/10V MLCC capacitor on the application board as close as possible to the VCC pin.

Register Descriptions

Register Address: 0x0A				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:0	REG_PRODUCT_ID<7:0>	00001000	R	Identify Device 00001000: AKM2800A 10011000: AKM2800B

Register Address: 0x0B				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:0	REG_CHIP_REV<7:0>	00000000	R	Silicon Revision

Register Address: 0x0C				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:0	REG_PVIN_ADC<7:0>	00000000	R	PVIN ADC Report LSB: 62.5mV Range: 0 to 15.9375V

Register Address: 0x0D				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:0	REG_VOUT_ADC<7:0>	00000000	R	VOUT ADC Report AKM2800A: LSB: 10mV, Range: 0.3 to 2.85V AKM2800B: LSB: 20mV, Range: 0.6 to 5.7V

Register Address: 0x0F				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:0	REG_TJ_ADC<7:0>	00000000	R	TJ ADC Report LSB: 1°C Range: -40°C to +150°C

Register Address: 0x10				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:0	REG_CRC_BYTE <7:0>	00000000	R	Checksum

Register Address: 0x12				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:1	RESERVED_12 <7:1>	0000000	RW	Reserved Bits
0	REG_VOS_REG<0>	1	RW	VOS Regulation MSB 100011000: 1.8V

Register Address: 0x13				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:0	REG_VOS_REG<7:0>	00011000	RW	VOS Regulation LSB 100011000: 1.8V

Register Address: 0x14				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:5	RESERVED_14<7:5>	000	RW	Reserved Bits
4:3	REG_SSTART_RATE<4:3>	00	RW	Soft Start Rate 00: 0.5mV/us (AKM2800A) 01: 1.0mV/us (AKM2800B) 10: 0.25mV/us 11: 2.0mV/us
2	REG_SW_SSTOP_EN	0	RW	Software Enable 0: Disable (default) 1: Enable
1	REG_DCM_ALLOW	0	RW	Allow DCM 0: Force CCM (default) 1: Allow DCM
0	REG_PG_CONTROL	1	RW	PG Control 0: DAC Based 1: Threshold Based (default)

Register Address: 0x15				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:2	RESERVED_15<7:2>	000000	RW	Reserved Bits
1:0	REG_CYC_OCP<1:0>	10	RW	Cycle OCP (valley) 00: 5A(AKM2800A) 2A (AKM2800B) 01: 6A (default AKM2800A) 3A (AKM2800B) 10: 4A(default AKM2800B) 11: 5A(AKM2800B)

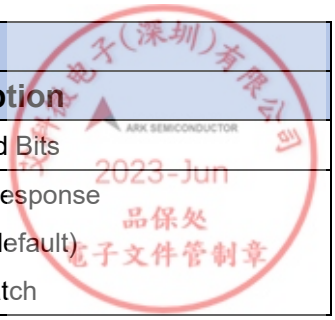
Register Address: 0x16				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:0	REG_BASE_ADDR<7:0>	00001000	RW	Base Address: 0x08

Register Address: 0x17				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:2	RESERVED_17<7:2>	000000	RW	Reserved Bits
1:0	REG_VOS_OVP<1:0>	11	RW	VOS OVP 00: 105% of VOS 01: 110% of VOS 10: 115% of VOS 11: 120% of VOS (default)

Register Address: 0x18				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:2	RESERVED_18<7:2>	000000	RW	Reserved Bits
1:0	REG_VOS_PG<1:0>	10	RW	VOS PG 00: 80% of VOS 01: 85% of VOS 10: 90% of VOS (default) 11: 95% of VOS

Register Address: 0x19				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:2	RESERVED_19<7:2>	000000	RW	Reserved Bits
1:0	REG_TJ_OTP<1:0>	11	RW	TJ OTP 00: 75 Degree 01: 85 Degree 10: 125 Degree 11: 145 Degree (default)

Register Address: 0x1A				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:1	RESERVED_1A<7:1>	0000000	RW	Reserved Bits
0	REG_VOS_OVP_RPS	0	RW	VOS OVP Response 0: Latch (default) 1: Unlatch



Register Address: 0x1C				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:4	RESERVED_1C<7:4>	0000	RW	Reserved Bits
3	REG_SW_SSTOP_CTL	0	RW	Software module control 0: Turn-off (default) 1: Turn-on
2:0	RESERVED_1C<2:0>	000	RW	Reserved Bits

Register Address: 0x1D				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:2	RESERVED_1D<7:2>	000000	RW	Reserved Bits
1	REG_EPROM_BURN_EN	0	RW	EPROM Burn Enable to burn the below register current value 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, 0x18, 0x19, 0x1A, 0x1C 0: Disable 1: Enable (default)
0	RESERVED_1D<0>	0	RW	Reserved Bits

Register Address: 0x1E				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7:6	RESERVED_1E<7:6>	00	R	Reserved Bits
5:3	STA_EPROM_LAST	000	R	Status Last EPROM Bank Burned 000: Last EPROM Bank0 Burned 001: Last EPROM Bank1 Burned 010: Last EPROM Bank2 Burned 100: Last EPROM Bank3 Burned 111: No Bank Burned
2:0	RESERVED_1E<2:0>	000	R	Reserved Bits

Register Address: 0x1F				
Bit	**Bit Name**	**Default**	**Type**	**Description**
7	STA_VOS_PG	0	R	Status VOS PG 0: Not Trigger 1: Yes Trigger
6	STA_VOS_OVP	0	R	Status VOS OVP 0: Not Trigger 1: Yes Trigger
5	STA_CYC_OCP	0	R	Status CYC OCP 0: Not Trigger 1: Yes Trigger
4	STA_TJ_OTP	0	R	Status TJ OTP 0: Not Trigger 1: Yes Trigger
3	STA_IO_EN	0	R	Status IO EN 0: Not Trigger 1: Yes Trigger
2	STA_EPROM_BURN	0	R	Status EPROM burning 0: Fail 1: Success
1:0	RESERVED_1F<1:0>	00	R	Reserved Bits

Application Circuit and BOM

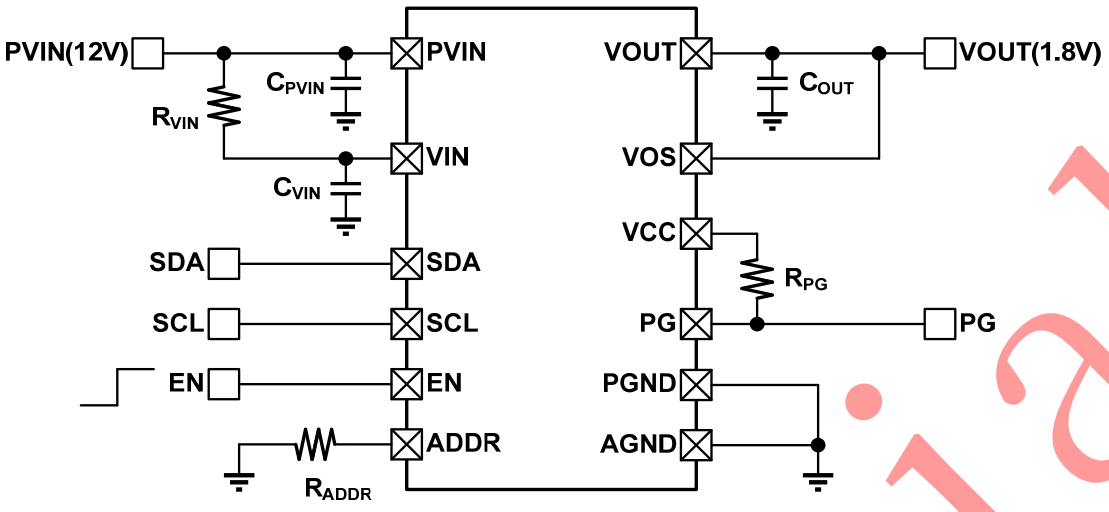


Figure 36 Application circuit for internal VCC supply

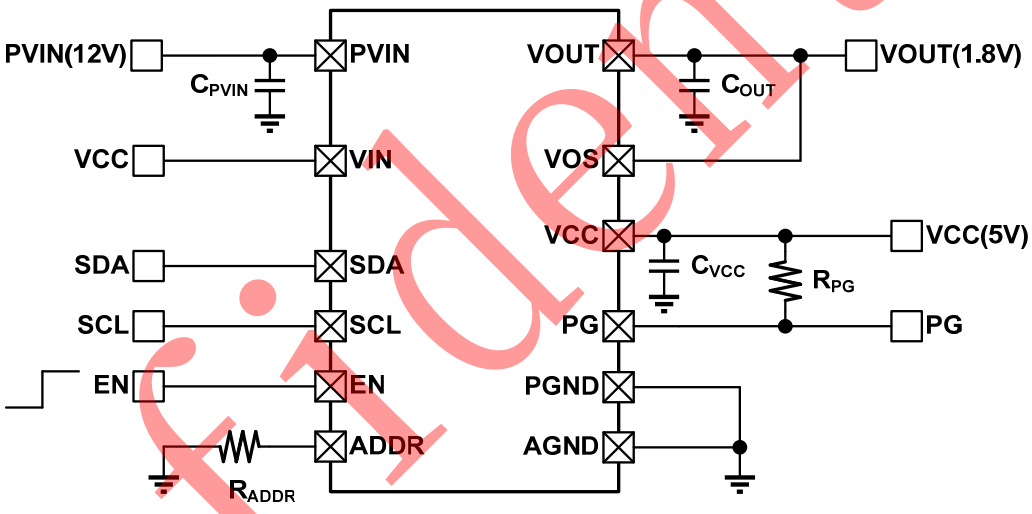


Figure 37 Application circuit for external VCC supply

Position	Description	Quantity
CPVIN	22uF/16V	≥ 2
CVIN	1uF/16V	1
CVCC	2.2uF/10V (option)	1
COUT	22uF/6.3V	≥ 3
R_{PG}	49.9KΩ	1
R_{ADDR}	0/10K/20K/30KΩ	1
R_{VIN}	2.7Ω	1

PCB layout guidelines

AKM2800 is a highly integrated device with very few external components, which simplifies PCB layout. However, for optimal performance, refer the guidelines below:

- PVIN and PGND traces should be as wide as possible to reduce trace impedance.
- PVIN to VIN traces add RC filter, reduce input voltage noise impedance.
- Output and input capacitors including PVIN, VIN and VCC bypass capacitor (if used) should be placed as close as possible to the AKM2800 pins.
- Output voltage should be sensed with a separated trace directly from the output capacitor.
- Analog ground and power ground are connected through a single-point connection.
- Place PGND vias (as many as possible and as close to PGND as possible) to minimize both parasitic impedance and thermal resistance.
- Output voltage feedback loop should be placed away from the high voltage switching trace, and preferably has ground shield.
- The trace of the VOS node should be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

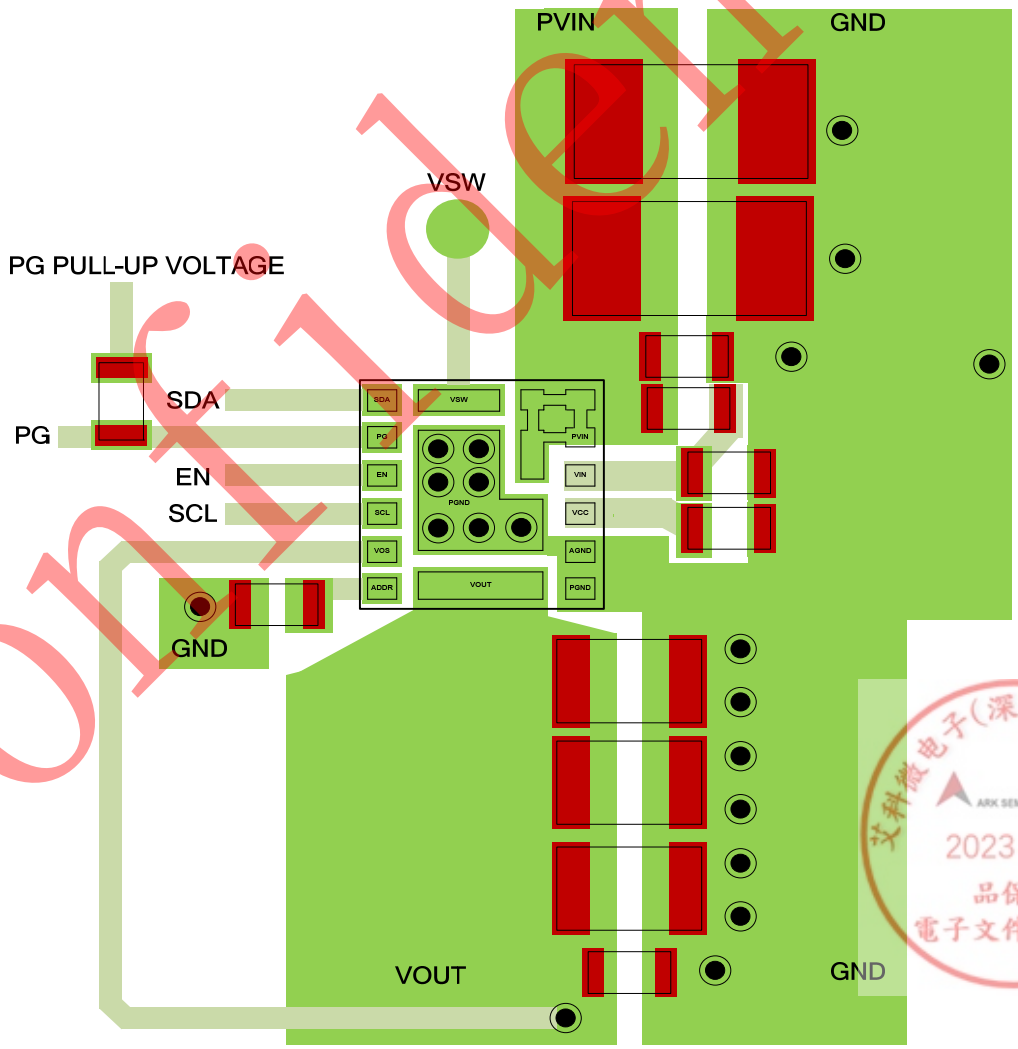


Figure 38 Recommended PCB layout

Reflow Parameters

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. *Figure 39* shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60~150 seconds limit to melt the solder and make the peak temperature at the range from 255°C to 260°C (Do not exceed 30 sec). It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

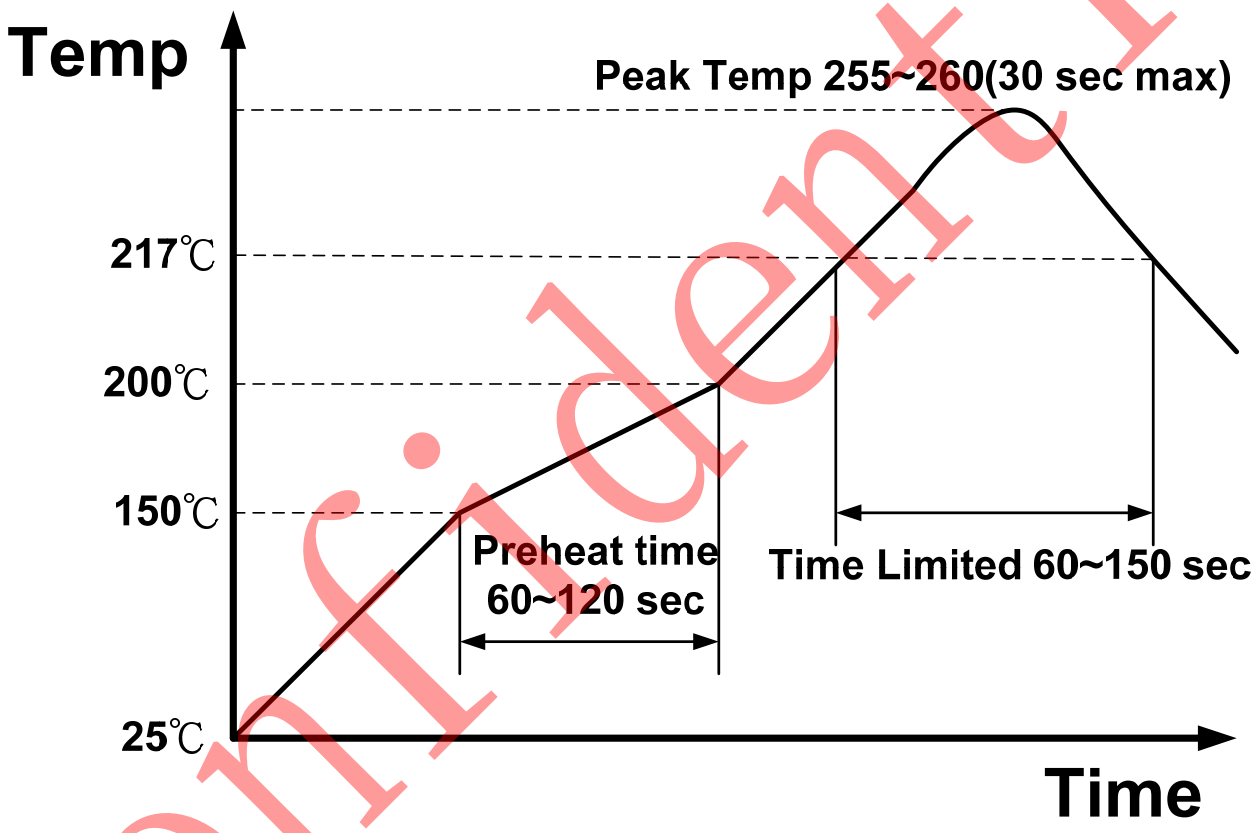


*Figure 39 Recommendation Reflow Profile**

*Refer to the Classification Reflow Profile of J-STD-020

Package Outline Drawing:

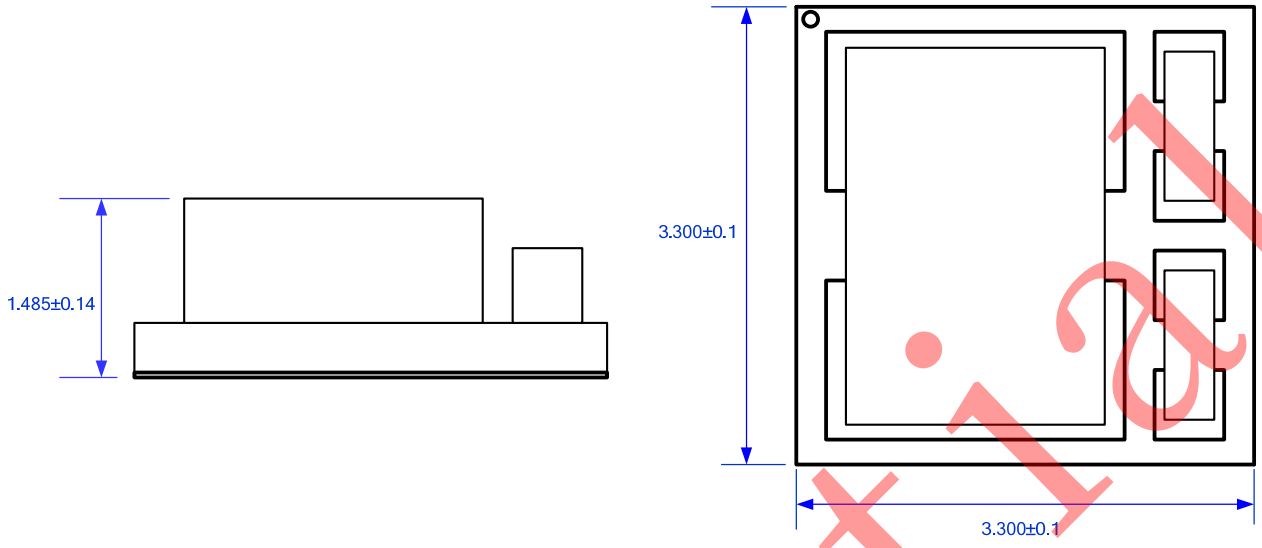


Figure 40 Side View and Top View

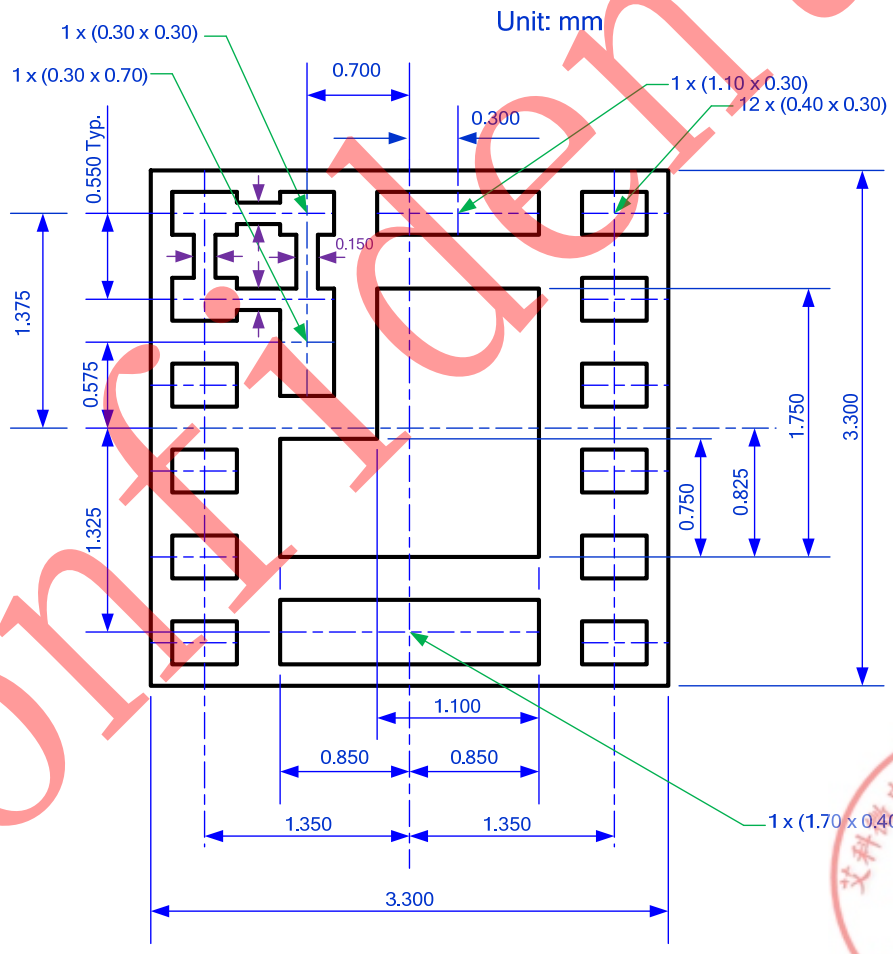
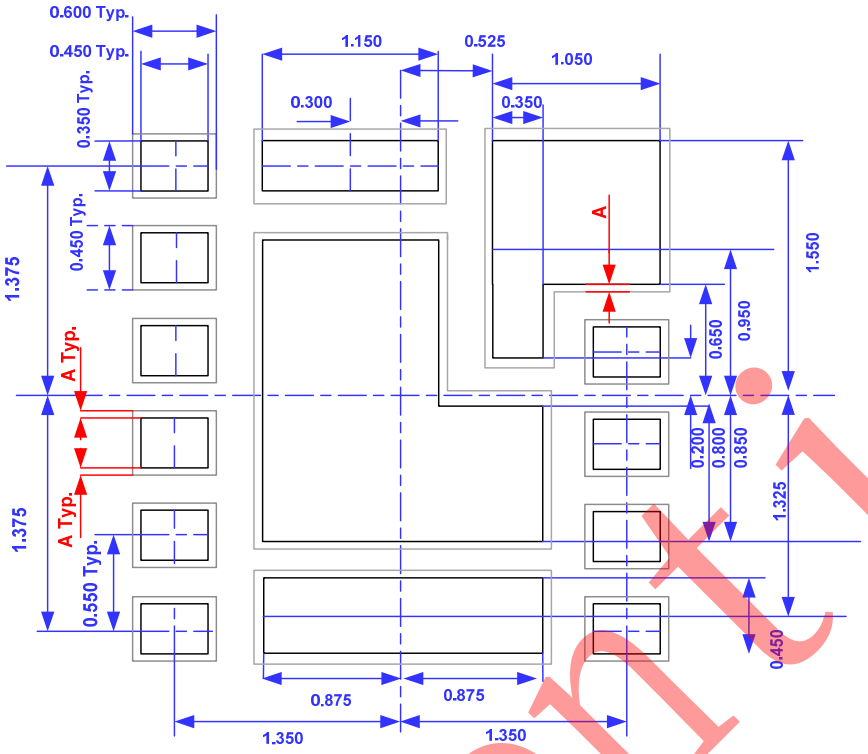


Figure 41 Bottom View

Land Pattern Reference:

Unit: mm



Copper pads are 25µm larger on each side than device footprint pads. Solder-mask openings are 75µm larger on each side than copper pads (50µm where marked 'A')

Figure 42 PCB layout

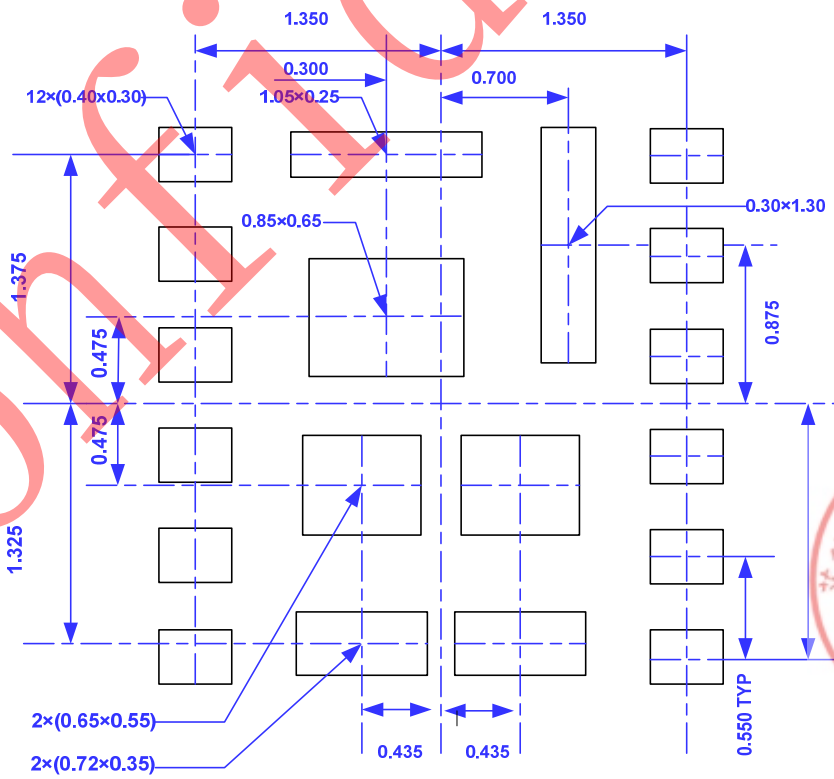


Figure 43 Solder stencil

Tape And Reel Information

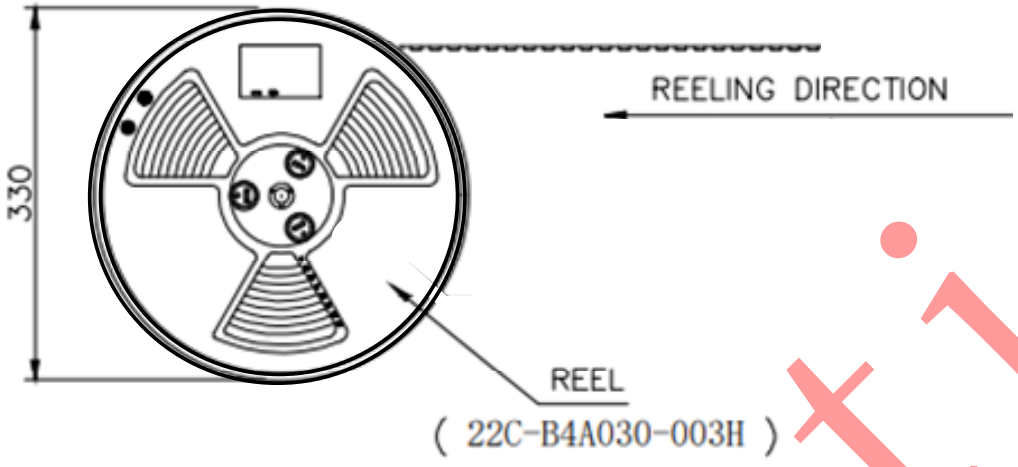


Figure 44 Reel Dimension

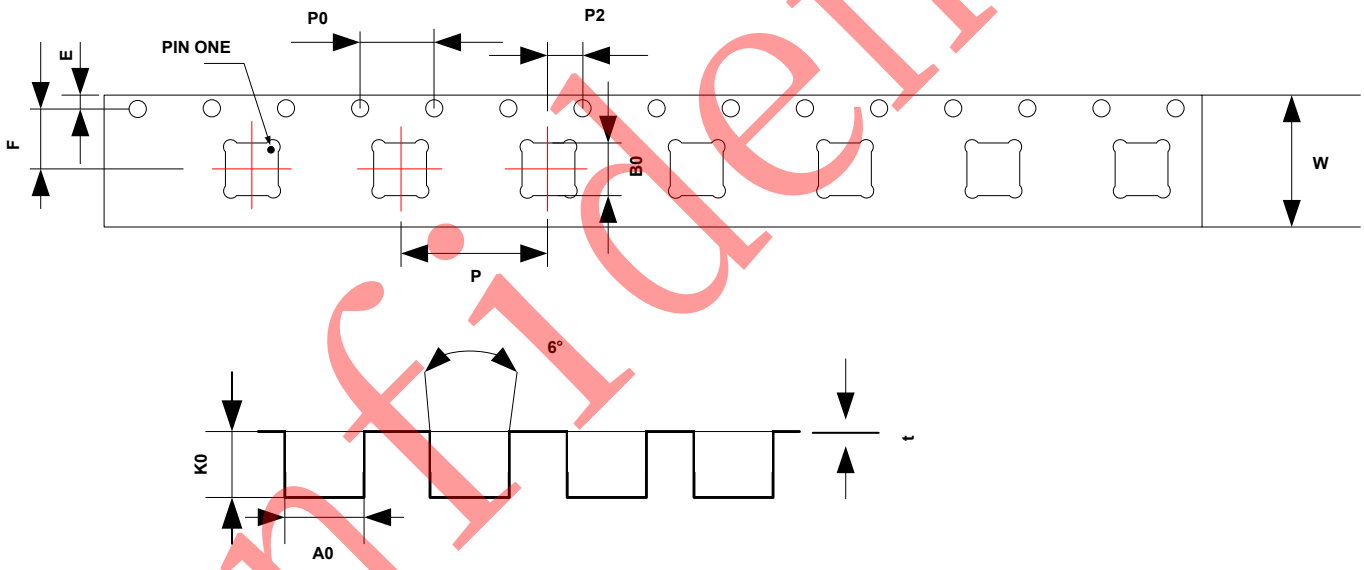


Figure 45 Tape Dimension

Item	DIM (mm)	
E	1.75	±0.1
F	5.50	±0.1
P2	2.00	±0.1
ΦD0	1.50	±0.1
P0	4.00	±0.1
10P0	40.00	±0.2
W	12.00	±0.3
P	8.00	±0.1
A0	3.50	±0.1
B0	3.50	±0.1
K0	2.50	±0.1
t	0.40	±0.05