EIM Technology

STEPFPGA(MXO2Core)

A simple & miniature FPGA development board

1. Features

STEPFPGA MXO2Core is a miniature FPGA development core board designed based on Lattice MXO2-4000 FPGA chip. The embedded components such as LEDs, segment displays, switches and pushbuttons help users tangibly interact and observe experimental results. The DIP40 footprint features the flexibility to expand projects on breadboard or embed the board for your products. STEPFPA MXO2Core is also extremely user friendly for FPGA beginners where you can develop lots of FPGA projects using our cloud-based Web IDE (Verilog) with simple interface and abundant pre-built examples.

2. General Functions

MXO2Core is small yet powerful. Figure 1 illustrated the components layout on the board and pin diagram definitions:

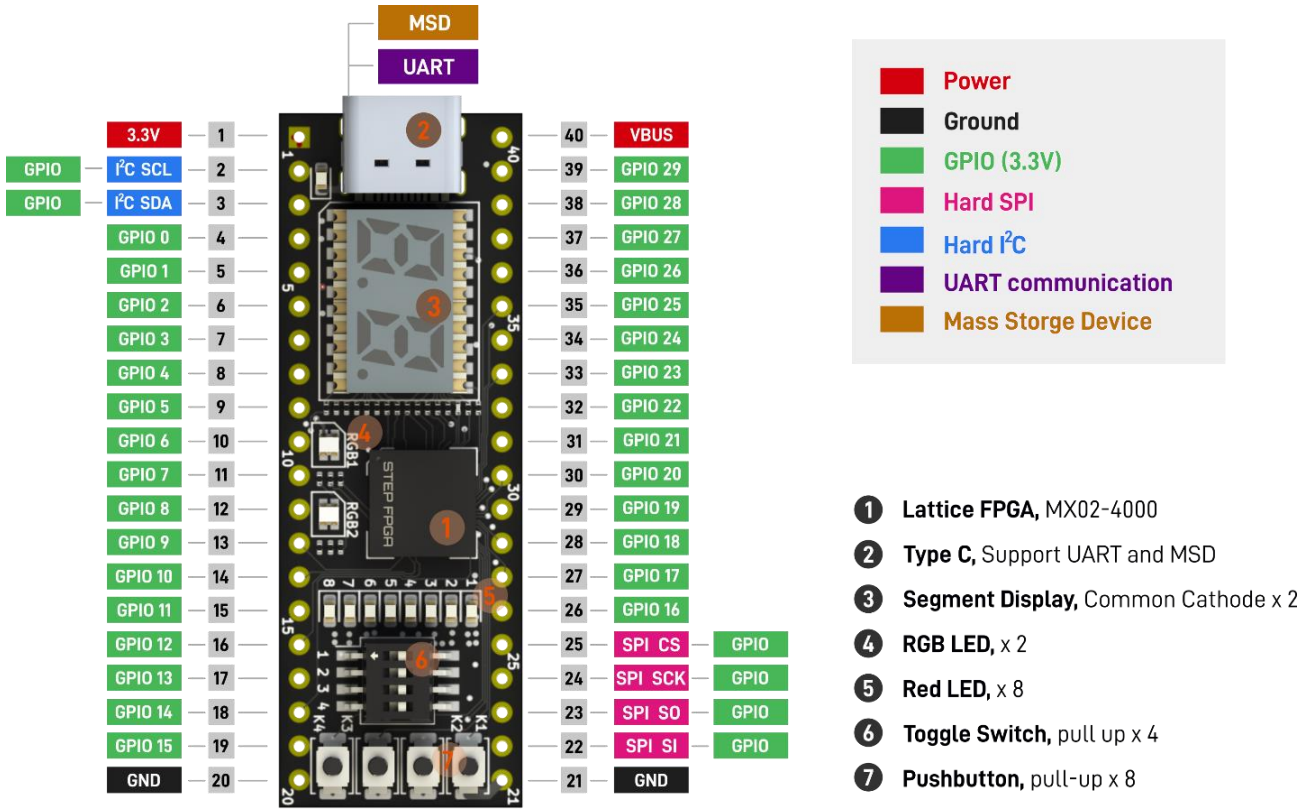


Figure 1: Overview of the board functionalities

For beginners, the MXO2Core board are good for implementation of fundamental digital circuits appeared in your curriculum textbooks such as Logic Gates, Decoders, Multiplexers, Flipflops, Counters…With the 36 GPIO pins and maximum of 400MHz clock frequency (boosted by the internal PLL), you can add many extension modules to explore advanced applications such as industrial controls, communications, signal processing and synthesis.

3. Technical Specifications

3.1 Board Overview

The hardware specifications of the board are summarized in Table 1.

Table 1: Hardware specs of the board

Board Name	STEPFPGA-MXO2Core
FPGA Chip	LCMXO2-4000HC
FPGA Manufacturer	Lattice Semiconductor
Resources	4320 LUTs
Block RAM	92Kbit
User Flash	64Kbit
GPIO (3.3V)	36
Hard IP-cores	SPI, I^2C, Timer
Supporting Soft cores	MICO8/32, 8051
IDE Tools	WebIDE, Diamond IDE
Burning Program	USB MSD (Flash drive)

3.2 Board Dimensions

The board has a Dual in-line package (DIP) footprint which can be directly plug fitting to a standard breadboard or larger motherboards for extension developments. The dimensions of board and layout of key components are outlined in Figure 2.

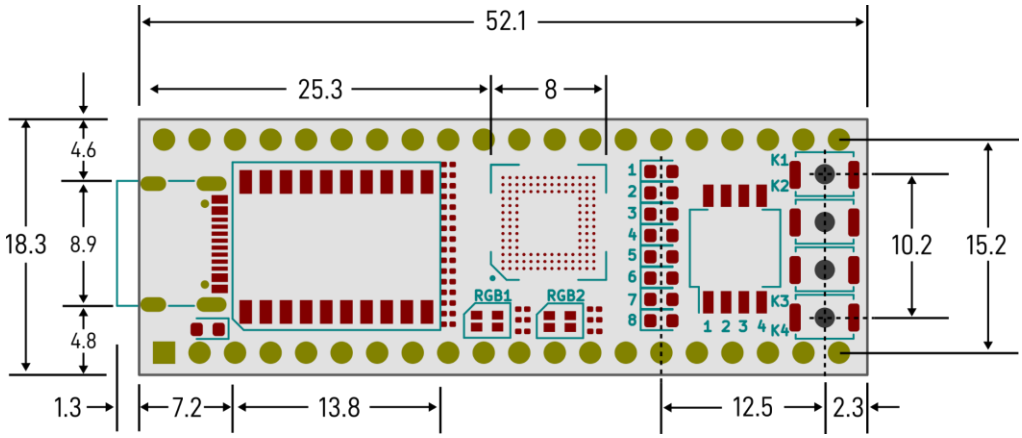


Figure 2: Board dimensions (in millimeters)

3.3 FPGA Pin Mapping

The pin-mapping diagram of STEPFPGA MXO2Core board is listed in Table2.

Table 2: Pin mapping diagram of STEPFPGA MXO2Core Board

GPIOs for Extension				On-board FPGA Pin Mapping			
GPIO PIN	FPGA PIN	GPIO PIN	FPGA PIN	Segment (Left)	FPGA PIN	UART	FPGA PIN
GPIO 1	3.3V	GPIO 40	VBUS	SEG-A1	A10	RXD	A2
						TXD	A3
GPIO 2	C8	GPIO 39	E12	SEG-B1	C11	Red LED	FPGA PIN
GPIO 3	B8	GPIO 38	F12	SEG-C1	F2	LED1	N13
GPIO 4	E3	GPIO 37	G12	SEG-D1	E1	LED2	M12
GPIO 5	F3	GPIO 36	F13	SEG-E1	E2	LED3	P12
GPIO 6	G3	GPIO 35	F14	SEG-F1	A9	LED4	M11
GPIO 7	H3	GPIO 34	G13	SEG-G1	B9	LED5	P11
GPIO 8	J2	GPIO 33	G14	SEG-DP1	F1	LED6	N10
GPIO 9	J3	GPIO 32	H12	SEG-DIG1	C9	LED7	N9
GPIO 10	K2	GPIO 31	J13	Segment (Right)	FPGA PIN	LED8	P9
GPIO 11	K3	GPIO 30	J14	SEG-A2	C12	Toggle	FPGA PIN
GPIO 12	L3	GPIO 29	K12	SEG-B2	B14	SW1	M7
GPIO 13	N5	GPIO 28	K14	SEG-C2	J1	SW2	M8
GPIO 14	P6	GPIO 27	K13	SEG-D2	H1	SW3	M9
GPIO 15	N6	GPIO 26	J12	SEG-E2	H2	SW4	M10
GPIO 16	P7	GPIO 25	P3	SEG-F2	B12	Pushbutton	FPGA PIN
GPIO 17	N7	GPIO 24	M4	SEG-G2	A11	K1	L14
GPIO 18	P8	GPIO 23	N4	SEG-DP2	K1	K2	M13
GPIO 19	N8	GPIO 22	P13	SEG-DIG2	A12	K3	M14
GPIO 20	GND	GPIO 21	GND	Crystal (12M)	FPGA PIN	K4	N14
				PCLK	C1		
• Maximum VBUS voltage is 6V • GPIO (High) = 3.3V • Segment display is Common Cathode				RGB (Left)	FPGA PIN	RGB (Right)	FPGA PIN
				R	M2	R	M3
				G	N2	G	N3
				B	P2	B	P4

Please note that if you set GPIOs as INPUT pins, they will be configured to internal pull-down structure by default.

4. Software Development Kit

There are two IDE tools available to develop the board. A recommended tool for FPGA beginners is the WebIDE tool for STEPFPGA, which is a cloud-based simplified tool integrated with all essential features to implement digital circuits.

WebIDE

To start, go to: www.eimtechnology.com and select for WebIDE as instructed in Figure 3.

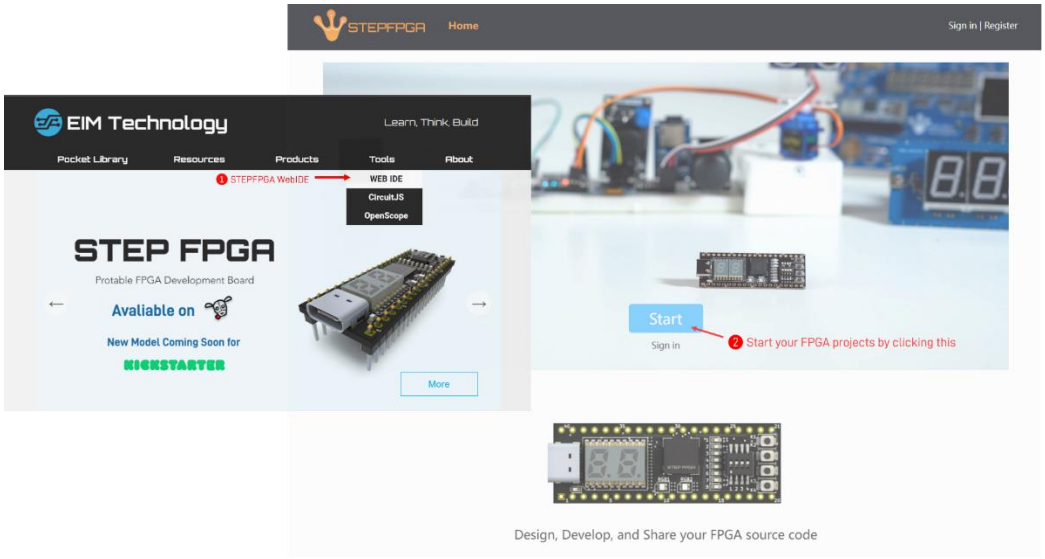


Figure 3: Acessing the WebIDE tool for STEPFPGA MXO2-Core board

Figure 4 shows the project creation page for which you need to name your project and select the hardware board used. Currently the IDE supports MXO2-Core (the one used in this tutorial) and MXO2-C (previous version that has no UART port).

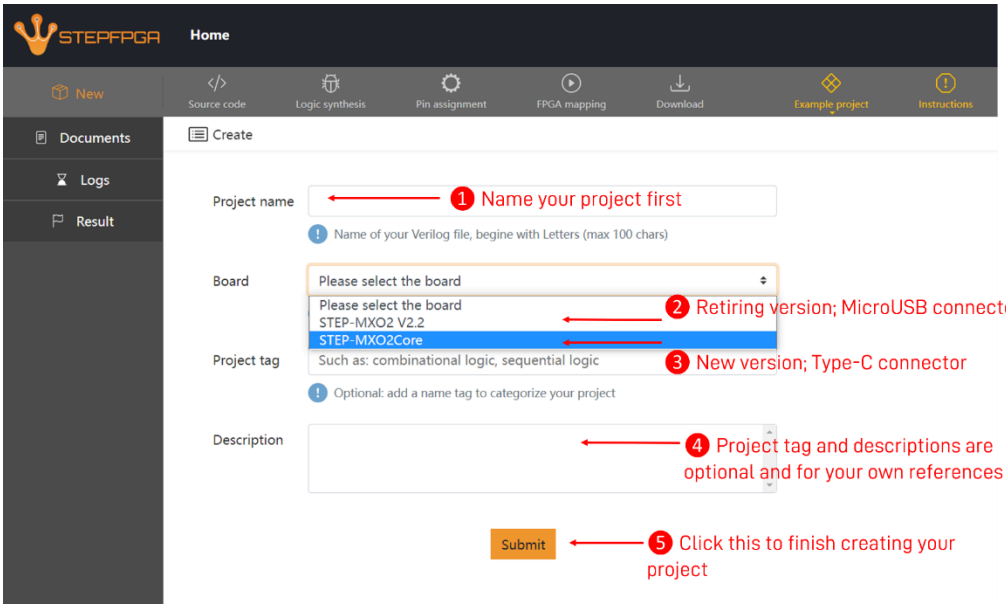
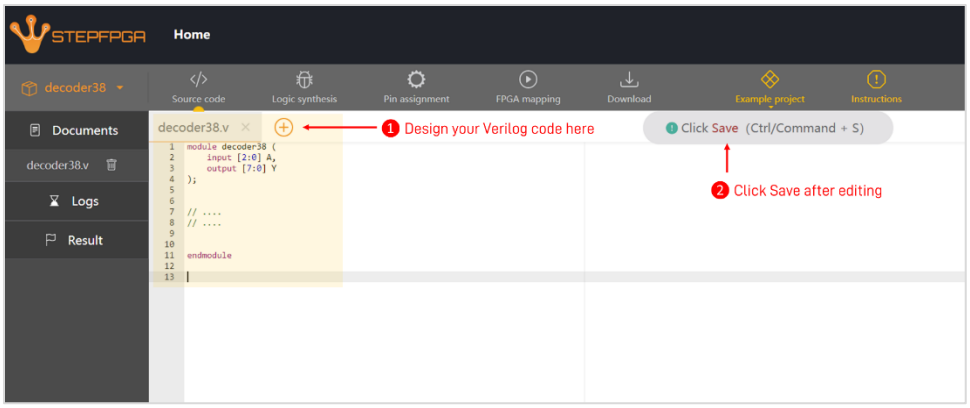


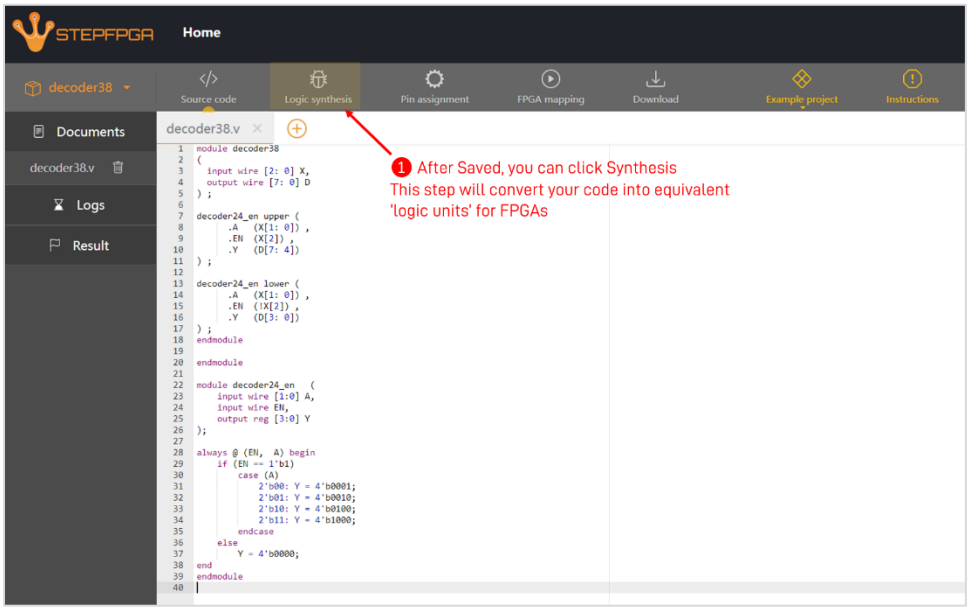
Figure 4: Creating a project on WebIDE

A detailed instruction of the WebIDE tool can be found at the top right ‘instructions’ canvas page, here we simply go over some important steps that converts a Verilog code into actual implementation file for STEPFPGA boards to execute.

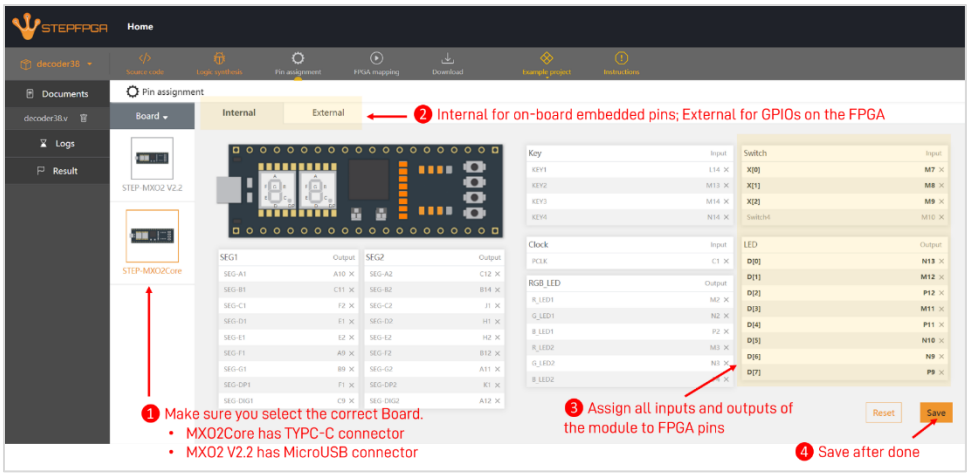
❶ Create the project file and complete the Verilog design code for the decoder38 module



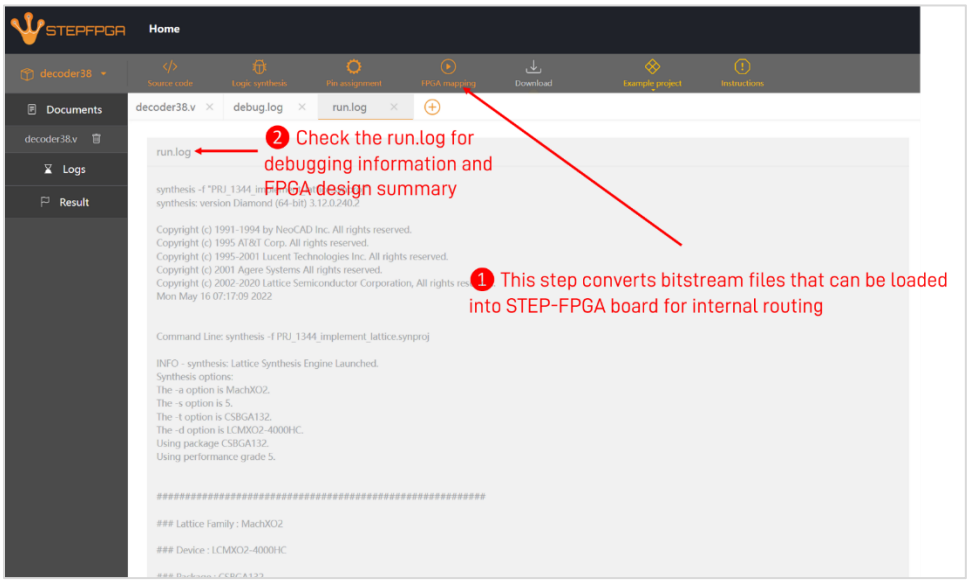
❷ If the code is correct, the compiler will be shown as successful.



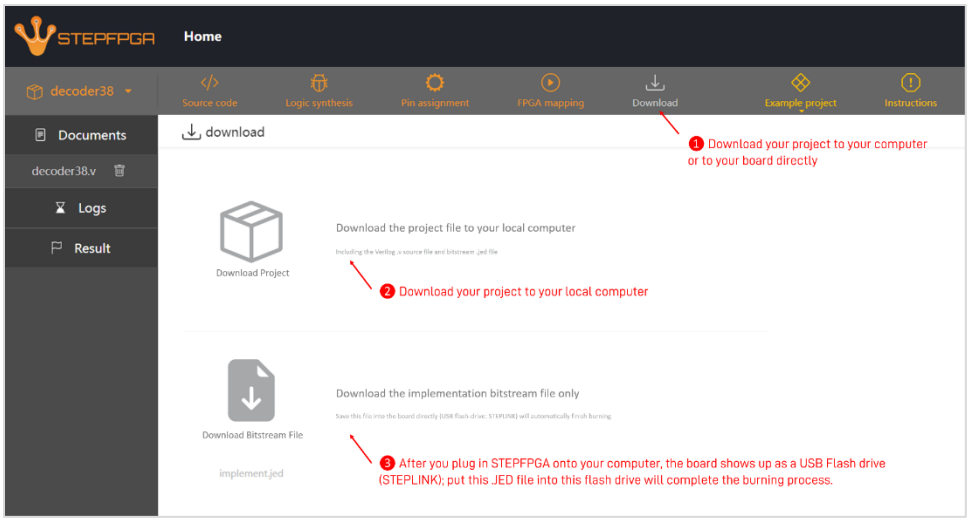
❸ Assign the input and output pins defined in the module to the corresponding ports of the small-pinma FPGA. Click Save after finishing the pin assignment.



❹ Map the above configurations into the corresponding FPGA internal alignments.



❺ When the mapping is successful, the IDE will generate the final hardware configuration file implementation.jed. Drag and drop the file directly into the Little Foot FPGA to complete all hardware configurations.



Diamond IDE

Find Diamond software in Lattice Semiconductor website download page, see Figure 5, then download and install.

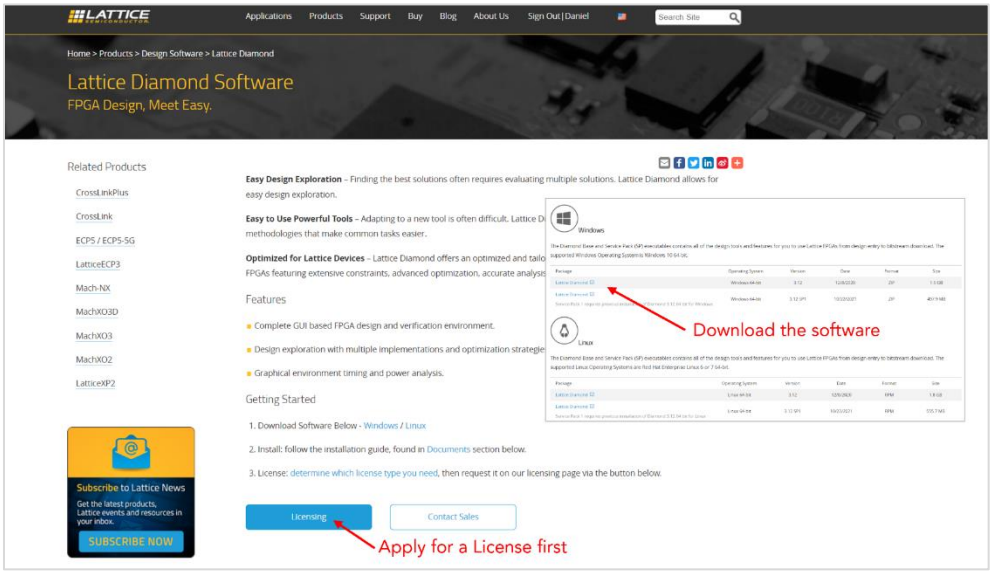


Figure 5: Login to the Lattice website to find the download file

After opening Diamond IDE, you will start off by creating a new project file, see Figure 6. Your project folder holds all work pieces including Verilog design files, simulation results and implementation files, so set the folder directory to a place that is easy to locate.

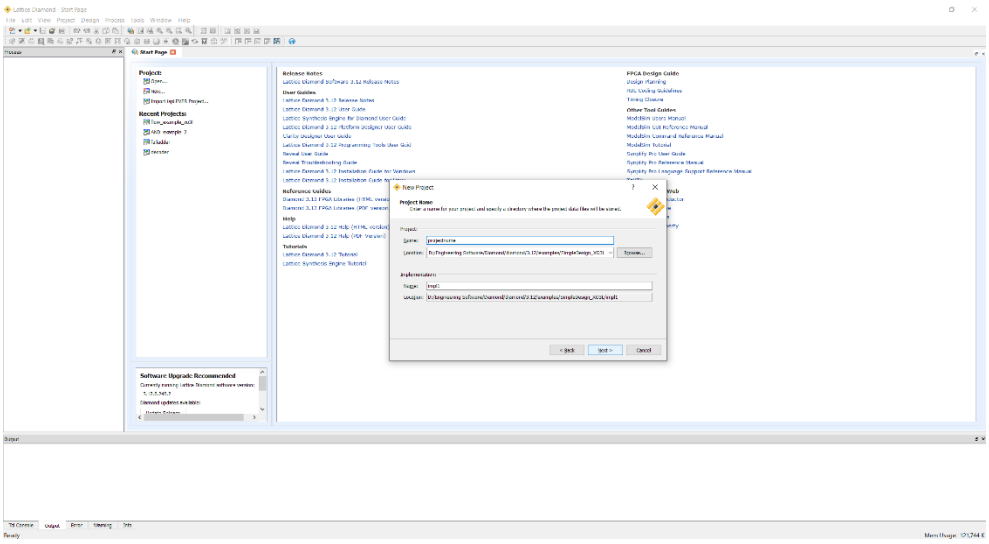


Figure 6: Creating an FPGA project in Diamond IDE

Then select “MXO2-4000HC” for the chip, see Figure 7.

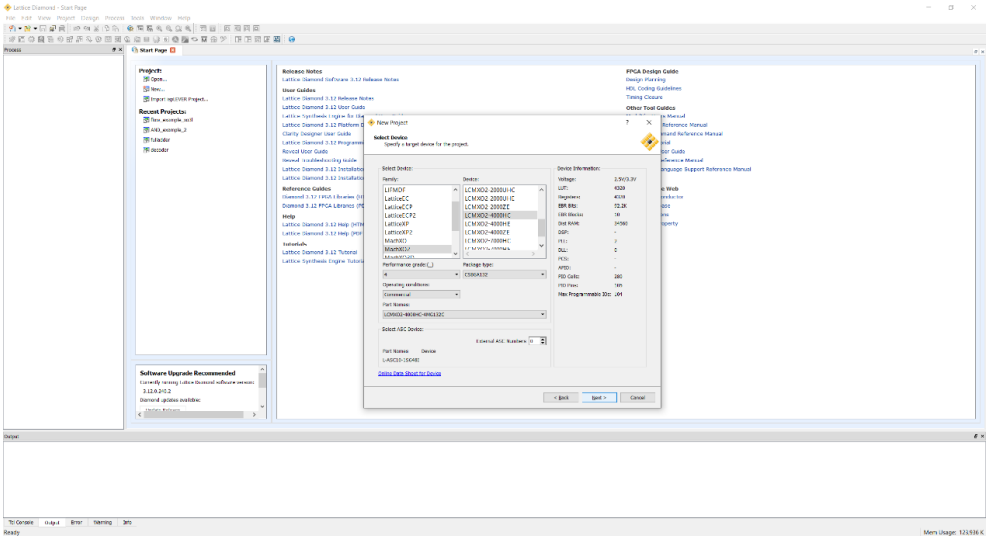


Figure 7: Selecting the corresponding board model

The development interface of Diamond looks like Figure 8, where you have different working areas for HDL design, EDA tools, output message area and file hierarchy.

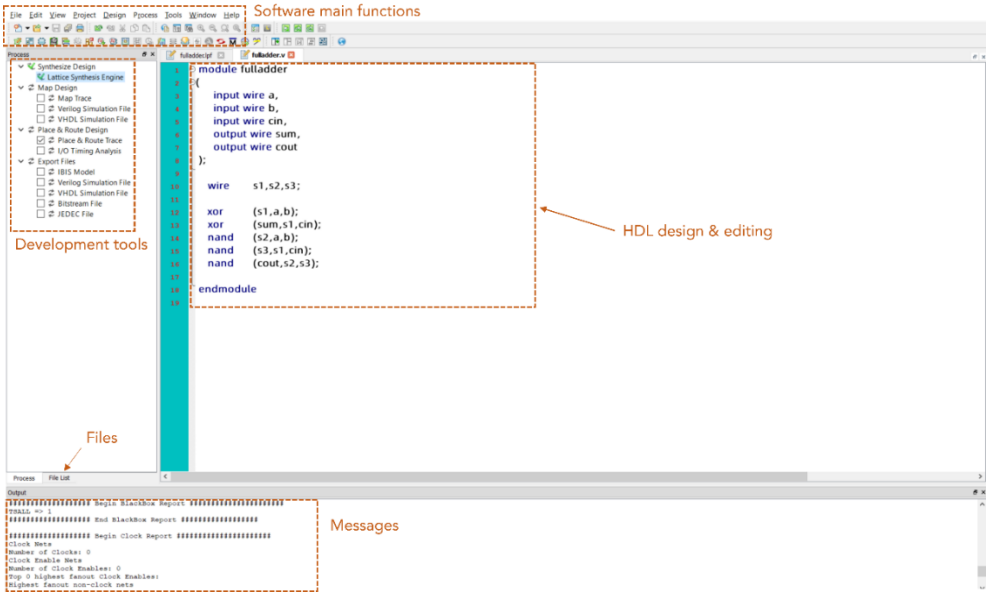


Figure 8: Introduction to the development interface

Once the Verilog design is completed, use the development EDA tools to continue the synthesize, pin mapping, place and route trace and eventually generate the implementation file. To assign inputs and outputs to FPGA IO pins, click ‘Spreadsheet View’ and assign pins accordingly as shown in Figure 9.

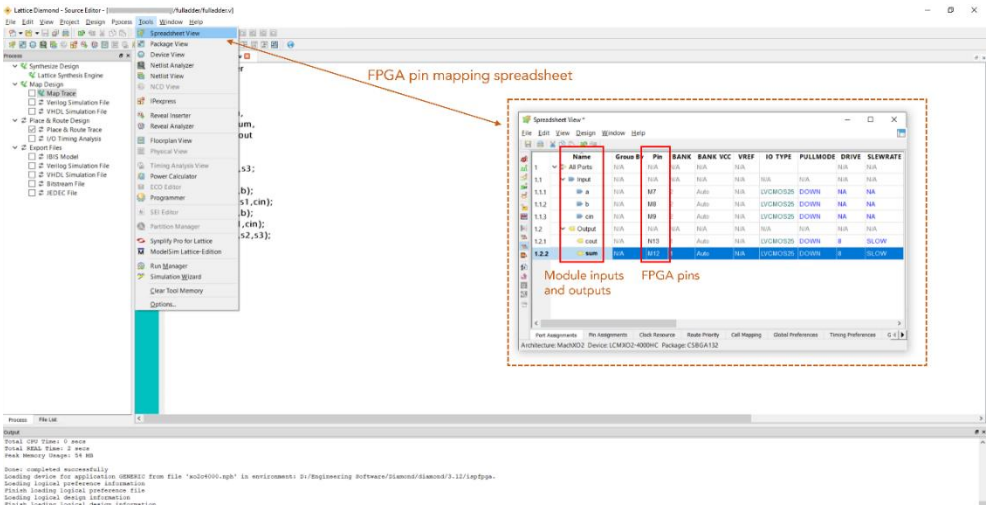


Figure 9: FPGA chip pin assignment

The implementation file generated by Diamond IDE has a file extension ‘.jed’, which can be programmed into the FPGA chip. When you plug this STEPFPGA board to your computer, it is automatically configured as a USB flash drive. To program the FPGA, you can simply drag the .jed file into this USB drive to complete the final programming.

5. Resources

Tutorials and relevant technical documentation are available and can be found at the Teaching Resource section of the website. Figure 10 is the cover page of the Alpha edition of the tutorial book, which was launched on Kickstarter in July 2022 as a learning guide. The official book edition is expected to be published on Amazon Kindle by the end of 2022.

Figure 10: Tutorial for FPGA Beginners

The codes in this book was open sourced at this link:

https://github.com/eimtechnology/STEPFPGA-MXO2Core/tree/main/Tutorial%20Level1

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