VL53L5CX

Datasheet

Time-of-Flight 8x8 multizone ranging sensor with wide field of view

Product status link
VL53L5CX

Features

- Fast and accurate multizone distance ranging sensor
  - Multizone ranging output with either 4x4 or 8x8 separate zones
  - Autonomous Low-power mode with interrupt programmable threshold to wake up the host
  - Up to 400 cm ranging
  - Multitarget detection and distance measurement in each zone
  - 60 Hz frame rate capability
  - Histogram processing and algorithmic compensation minimizes or removes impact of cover glass crosstalk
  - Motion indicator for each zone to show if targets have moved and how they have moved
- Fully integrated miniature module with wide field of view (FoV)
  - Emitter: 940 nm invisible light vertical cavity surface emitting laser (VCSEL) and integrated analog driver
  - 63 ° diagonal square FoV using diffractive optical elements (DOE) on both transmitter and receiver
  - Receiving array of single photon avalanche diodes (SPADs)
  - Low-power microcontroller running Firmware
  - Size: 6.4 x 3.0 x 1.5 mm
- Easy integration
  - Single reflowable component
  - Flexible power supply options, single 3.3 V or 2.8 V operation or combination of either 3.3 V or 2.8 V AVDD with 1.8 V IOVDD
  - Compatible with wide range of cover glass materials

Applications

- Scene understanding. Multizone and multi-object distance detection enables 3D room mapping and obstacle detection for robotics applications
- Wide FoV and multizone scanning allows content management (load in trucks, tanks, waste bins)
- Gesture recognition
- Liquid level control
- Keystone correction for video projectors
- Laser assisted autofocus (LAF). Enhances the camera AF system speed and robustness especially in difficult low light or low contrast scenes
- Augmented reality/virtual reality (AR/VR) enhancement. Dual camera stereoscopy and 3D depth assistance thanks to multizone distance measurement
- Smart buildings and smart lighting (user detection to wake up devices)
- IoT (user and object detection)
- Video focus tracking. 60 Hz ranging allows optimization of continuous focus algorithm

Description

The VL53L5CX is a state of the art, Time-of-Flight (ToF), multizone ranging sensor enhancing the ST FlightSense product family. Housed in a miniature reflowable package, it integrates a SPAD array, physical infrared filters, and diffractive optical elements (DOE) to achieve the best ranging performance in various ambient lighting conditions with a range of cover glass materials.

The use of a DOE above the vertical cavity surface emitting laser (VCSEL) allows a square FoV to be projected onto the scene. The reflection of this light is focused by the receiver lens onto a SPAD array.

Unlike conventional IR sensors, the VL53L5CX uses ST's latest generation, direct ToF technology which allows absolute distance measurement whatever the target color and reflectance. It provides accurate ranging up to 400 cm and can work at fast speeds (60 Hz), which makes it the fastest, multizone, miniature ToF sensor on the market.

Multizone distance measurements are possible up to 8x8 zones with a wide 63 ° diagonal FoV which can be reduced by software

Thanks to ST Histogram patented algorithms, the VL53L5CX is able to detect different objects within the FoV. The Histogram also provides immunity to cover glass crosstalk beyond 60 cm.

1 Product overview

1.1 Technical specifications

Table 1. Technical specifications

Feature	Details
Package	Optical LGA16
Size	6.4 x 3.0 x 1.5 mm
Ranging	2 to 400 cm per zone
Operating voltage	IOVDD: 1.8 or 2.8 V or 3.3 V AVDD: 2.8 V or 3.3 V
Operating temperature	-30 to 85 °C
Sample rate	Up to 60 Hz
Infrared emitter	940 nm
I^2C interface	I^2C: 400 kHz to 1 MHz serial bus, address: 0x52
Operating ranging mode	Continuous or Autonomous (see UM2884 for more information)

1.2 Field of view

Rx (or collector) exclusion zone includes all modules assembly tolerances and is used to define the cover window dimensions. The cover window opening must be equal to or wider than the exclusion zone.

The detection volume represents the applicative or system FoV in which a target is detected, and a distance measured. It is determined by the Rx lens or the Rx aperture, and is narrower than the exclusion zone.

Figure 1. System FoV and exclusion zone description (not to scale)

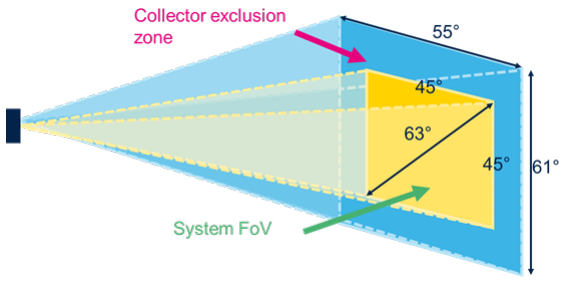


Table 2. FoV angles

	Horizontal	Vertical	Diagonal
Detection volume	45 °	45 °	63 °
Collector exclusion zone	55.5 °	61 °	82 °

Note: Detection volume depends on the environment and sensor configuration as well as target distance, reflectance, ambient light level, sensor resolution, sharpener, ranging mode, and integration time.

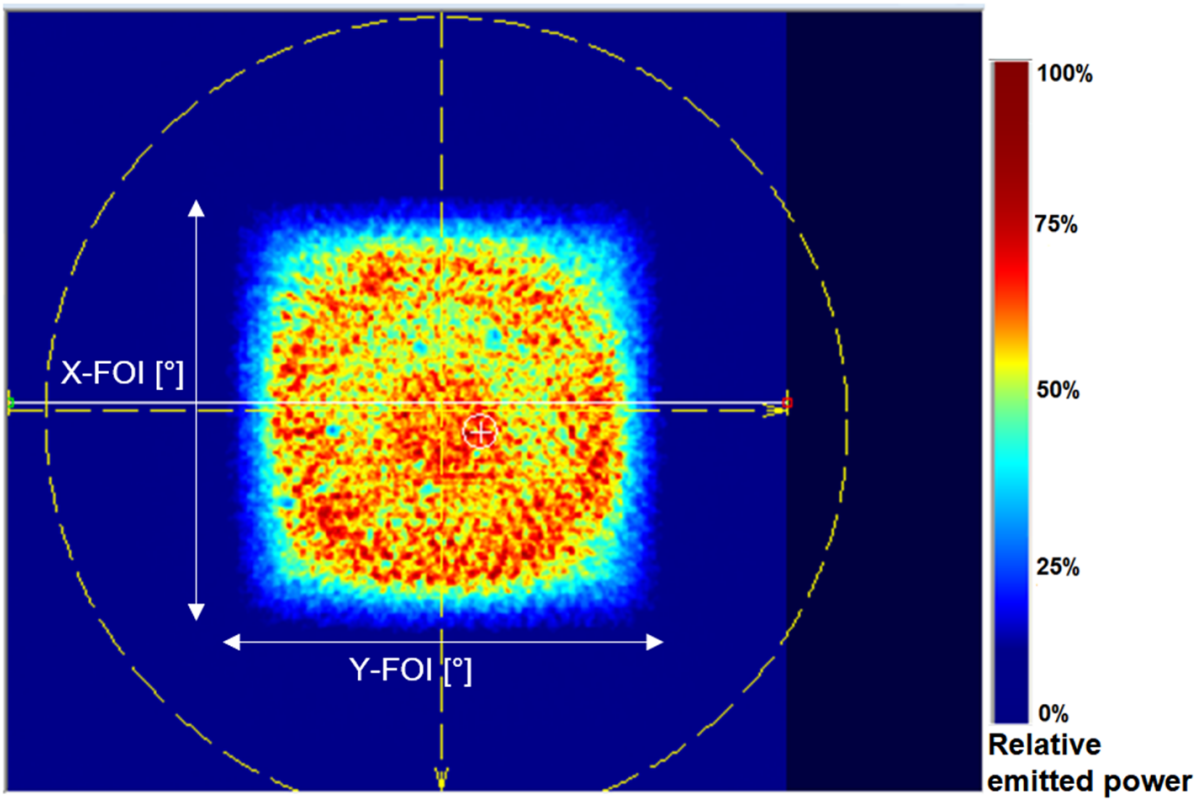
Note: The detection volume of Table 2. FoV angles has been measured with a white 88 % reflectance perpendicular target in full FoV, located at 1 m from the sensor, without ambient light (dark conditions), with an 8x8 resolution and 14 % sharpener (default value), in Continuous mode at 15 Hz.

1.3 Field of illumination

The VCSEL field of illumination (FoI) is shown in the figure below. The relative emitted signal power depends on the FoI angle, and corresponds to:

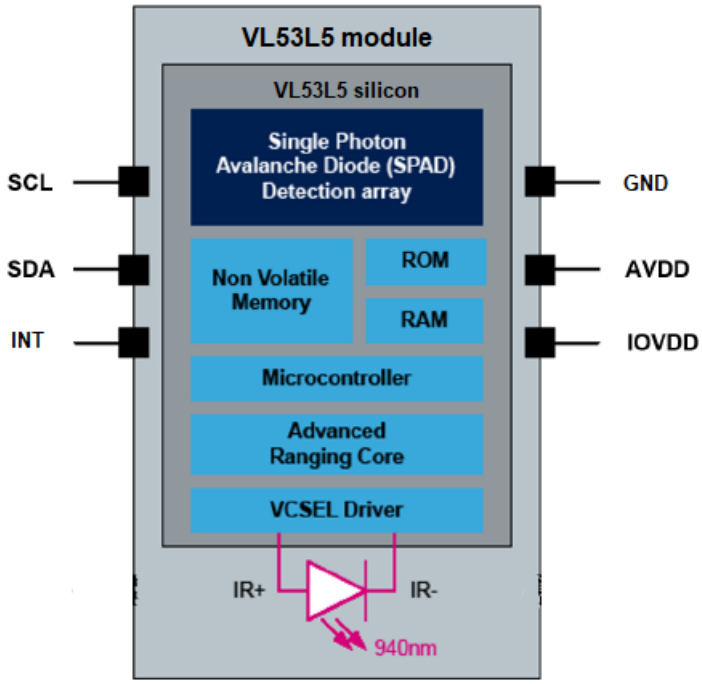
- 50 ° x 50 ° considering a beam with 75 % signal from maximum
- 65 ° x 65 ° considering a beam with 10 % signal from maximum

Figure 2. **VL53L5CX FoI**



1.4 System block diagram

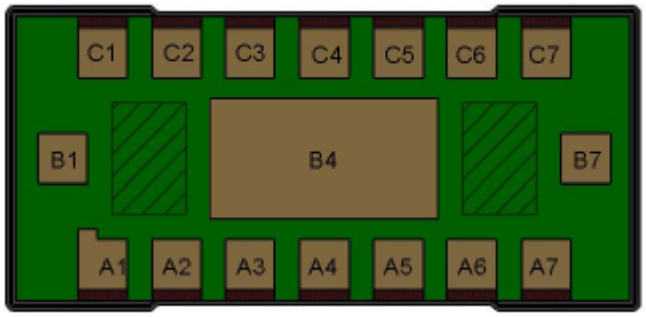
Figure 3. **VL53L5CX block diagram**



1.5 Device pinout

The figure below shows the pinout of the VL53L5CX

Figure 4. **VL53L5CX pinout (bottom view)**



The VL53L5CX pin description is given in the table below.

Table 3. VL53L5CX pin description

Pin number	Signal name	Signal type	Signal description
A1	I2C_RST	Digital input	I^2C interface reset pin, active high. Toggle this pin from 0 to 1, then back to 0 to reset the I^2C slave. Connect to GND via 47 kΩ resistor.
A2	RSVD4	Reserved	Connect to ground
A3	INT	Digital input/output (I/O)	Interrupt output, defaults to opendrain output (tristate), 47 kΩ pullup resistor to IOVDD required
A4	IOVDD	Power	1.8 V, 2.8 V or 3.3 V supply for digital core and I/O supply
A5	LPn	Digital input	Comms enable. Drive this pin to logic 0 to disable the I^2C comms when the device is in LP mode. Drive this pin to logic 1 to enable I^2C comms in LP mode. Typically used when it is required to change the I^2C adress in multidevice systems. A 47 kΩ pullup resistor to IOVDD is required.
A6	RSVD1	Reserved	Connect to ground
A7	RSVD2	Reserved	Connect to ground
B1	AVDD	Power	2.8 V or 3.3 V analog and VCSEL supply
B4	THERMALPAD	Ground	Connect to a ground plane to allow good thermal conduction
B7	AVDD	Power	2.8 V or 3.3 V analog and VCSEL supply
C1	GND	Ground	Ground
C2	RSVD6	Reserved	General purpose I/O, defaults to opendrain output (tristate), 47 kΩ pullup resistor to IOVDD required
C3	SDA	Digital I/O	Data (bidirectional), 2.2 kΩ pullup resistor to IOVDD required
C4	SCL	Digital input	Clock (input), 2.2 kΩ pullup resistor to IOVDD required
C5	RSVD5	Reserved	Do not connect
C6	RSVD3	Reserved	Connect to ground
C7	GND	Ground	Ground

Note: The THERMALPAD pin has to be connected to ground (for more information refer to AN5657).

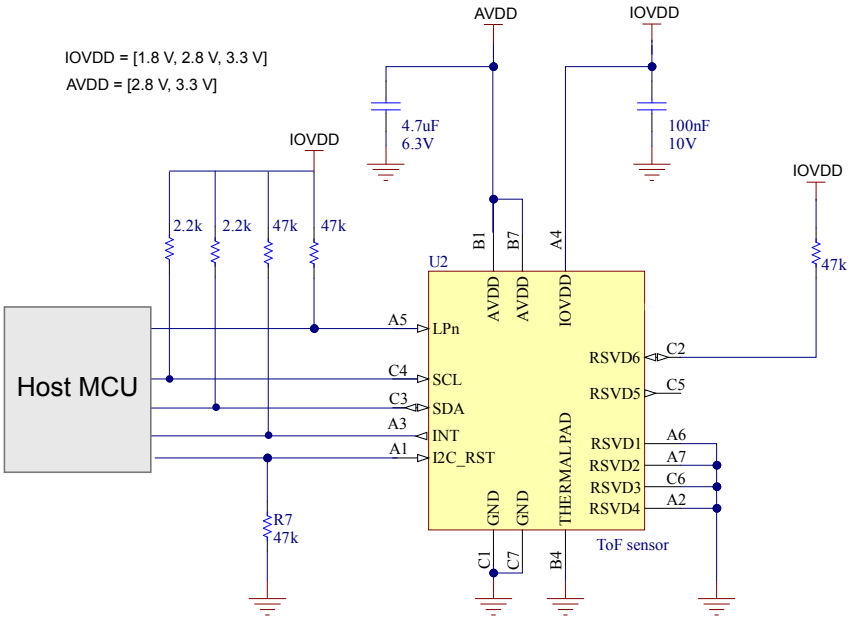
Note: All digital signals must be driven to the IOVDD level.

Note: Toggling the I2C_RST pin resets the sensor I2C communication only. It does not reset the sensor itself. To reset the sensor please refer to the sensor reset management procedure (UM2884).

1.6 Application schematic

The figures below show the application schematic of the VL53L5CX with different IOVDD and AVDD combinations.

Figure 5. Typical application schematic



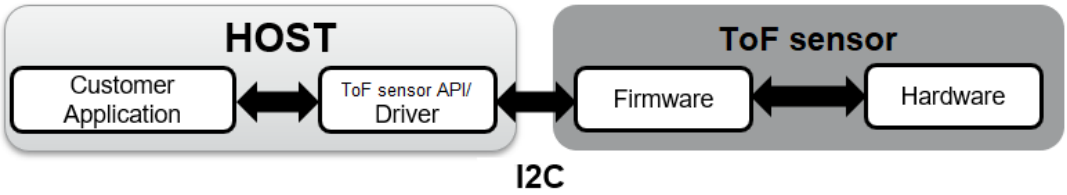
Note: Capacitors on the external supplies (AVDD and IOVDD) should be placed as close as possible to the module pins.

2 Functional description

2.1 Software interface

This section shows the software interface of the device. The host customer application controls the VL53L5CX using an application programming interface (API). The API implementation is delivered to the customer as a driver (C code and reference Linux driver). The driver provides the customer application with a set of high level functions that allow control of the VL53L5CX Firmware such as device initialization, ranging start/stop, mode select etc.

Figure 6. VL53L5CX system functional description



2.2 Power state machine

Figure 7. Power state machine

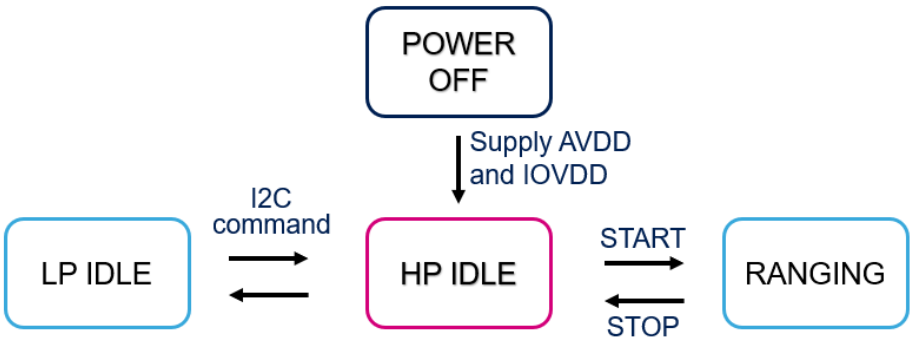


Table 4. Power state description

Device state	Description
LP idle	Low power idle state with data retention RAM and register content retained Allows fast resume to HP idle I^2C communication disabled if using LPn
HP idle	High power idle state Device needs to be in HP idle state to start ranging Power up state
Ranging	Full operation VCSEL is active (pulsing)

2.3 Power up sequence

The recommended power up sequence is shown in the figure below. When powering up the device, the IOVDD supply should be applied at the same time or after AVDD. When removing power, the AVDD supply should be removed at the same time or after IOVDD.

Note: Avoid powering IOVDD while AVDD is unpowered to prevent increased leakage current.

Figure 8. Power up sequence

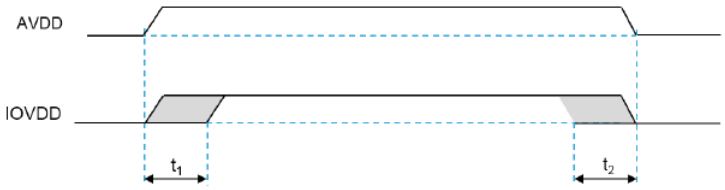


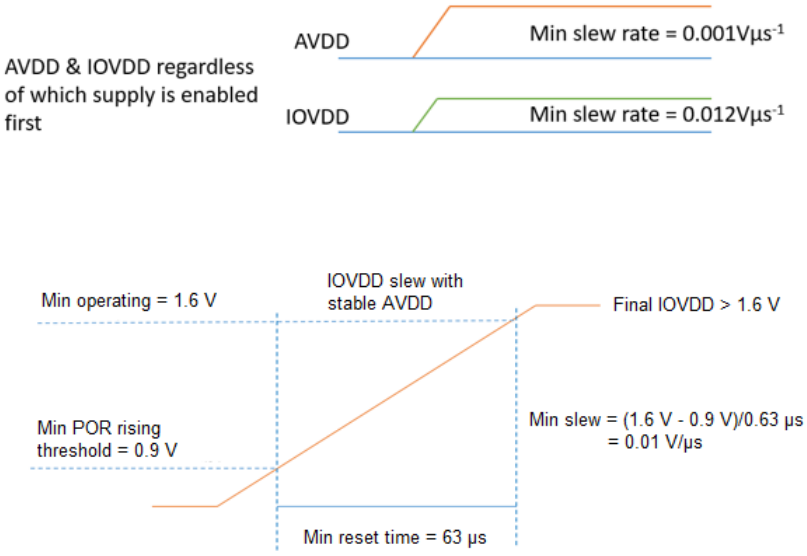
Table 5. Power up timing table

Time	Description	Min.
t_1	IOVDD rise after AVDD	0 s
t_2	IOVDD fall before AVDD	0 s

2.3.1 Power up slew

To ensure proper operation of the module, the following minimum slew rates on the supplies must be met for correct operation of the power on reset (POR) circuitry. The POR circuitry triggers at 0.9 V, but the supplies should reach their operation levels in accordance with the slew rates listed in the table below.

Figure 9. Power up slew



Note: The minimum reset time is the minimum time required for the device ROM to load and boot up after IOVDD reaches the POR rising threshold. The supply must have reached the minimum operating level (1.6 V) within this time.

Note: The minimum slew rate on the IOVDD is the same regardless of 1.8 V or 2.8 V operation.

Note: The AVDD rise time is determined by the internal analogue levels which must be stable for correct operation.

Table 6. Supply slew rate minimum limits

Supply status	AVDD slew	IOVDD slew
Start together	0.001 V/µs	0.012 V/µs
AVDD stable followed by IOVDD	—	0.012 V/µs
IOVDD stable followed by AVDD	0.001 V/µs	—

2.3.2 Power up and I²C access

For correct operation of the device, the I²C interface assumes the power level has reached 1.62 V.

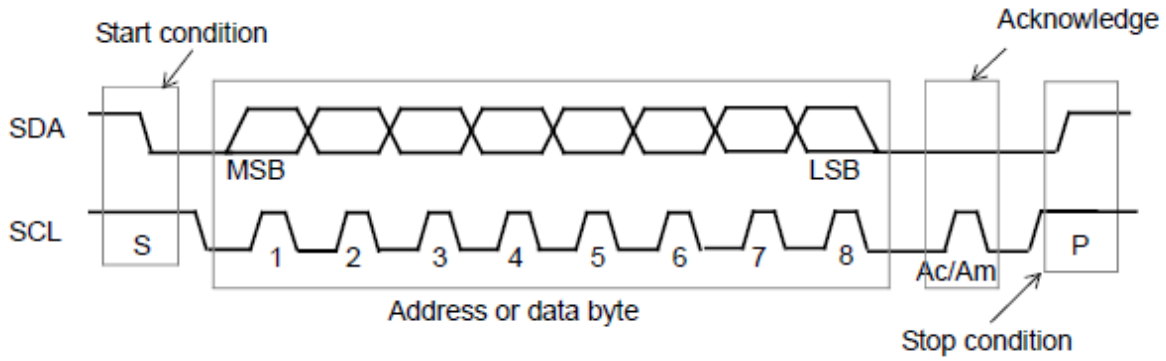
3 I²C control interface

This section specifies the control interface. The I²C interface uses two signals: serial data line (SDA) and serial clock line (SCL). Each device connected to the bus uses a unique address and a simple master / slave relationships exists.

Both SDA and SCL lines are connected to a positive supply voltage using pull-up resistors located on the host. Lines are only actively driven low. A high condition occurs when lines are floating and the pull-up resistors pull lines up. When no data is transmitted both lines are high.

Clock signal (SCL) generation is performed by the master device. The master device initiates data transfer. The I²C bus on the VL53L5CX has a maximum speed of 1 Mbits/s and uses a device 8-bit address of 0x52.

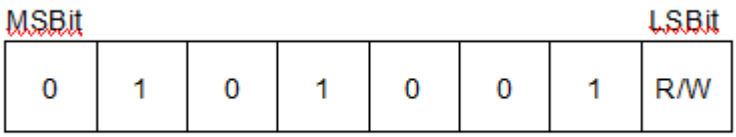
Figure 10. Data transfer protocol



Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit, Ac for VL53L5CX acknowledge and Am for master acknowledge (host bus master). The internal data are produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

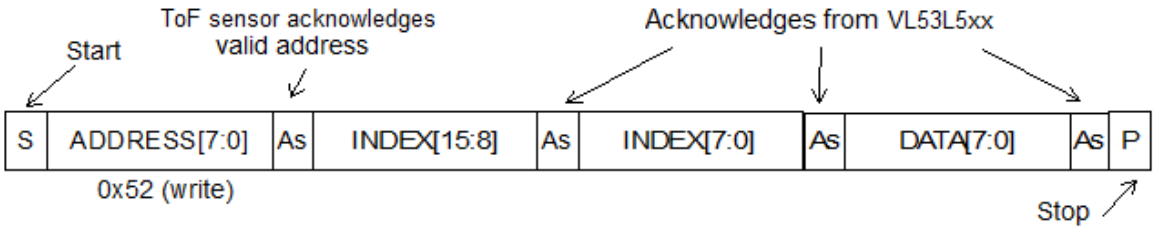
A message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition but without a preceding stop condition) followed by another message. The first byte contains the device address (0x52) and also specifies the data direction. If the least significant bit is low (that is, 0x52) the message is a master-write-to-the-slave. If the lsb is set (that is, 0x53) then the message is a master-read-from-the-slave.

Figure 11. VL53L5CX I²C device address: 0x52



All serial interface communications with the camera module must begin with a start condition. The VL53L5CX module acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/write bit (lsb of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted. During a write sequence, the second byte received provides a 16-bit index which points to one of the internal 8-bit registers.

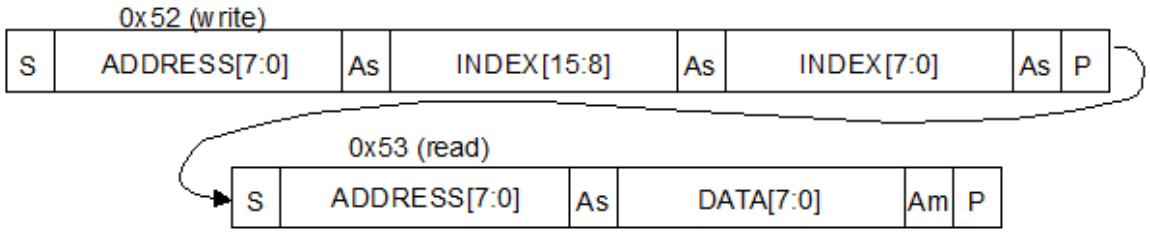
Figure 12. **VL53L5CX data format (write)**



As data are received by the slave, they are written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data are then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index is read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 13. **VL53L5CX data format (read)**



At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the VL53L5CX for a write and the host for a read).

A message can only be terminated by the bus master, either by issuing a stop condition or by a negative acknowledge (that is, not pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports auto-increment indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a stop condition. If the auto-increment feature is used the master does **not** have to send address indexes to accompany the data bytes.

Figure 14. **VL53L5CX data format (sequential write)**

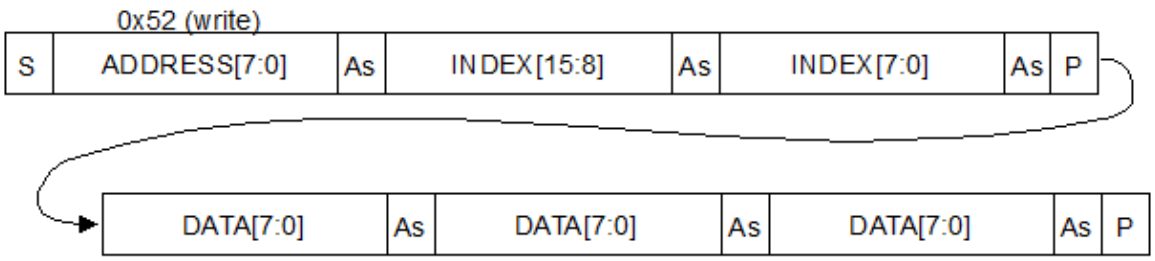
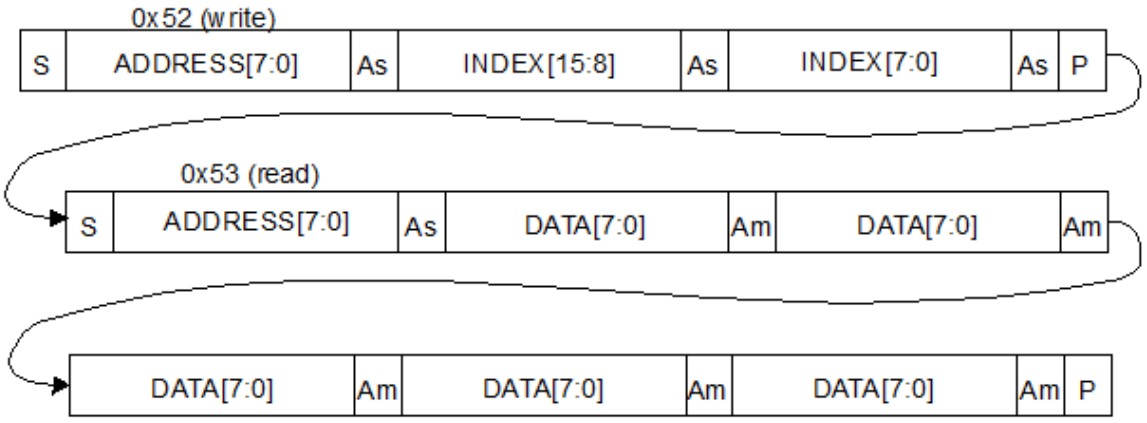


Figure 15. **VL53L5CX data format (sequential read)**



3.1 I²C interface - timing characteristics

Timing characteristics are shown in the tables below. Please refer to the figure below for an explanation of the parameters used.

Timings are given for all process, voltage and temperature (PVT) conditions.

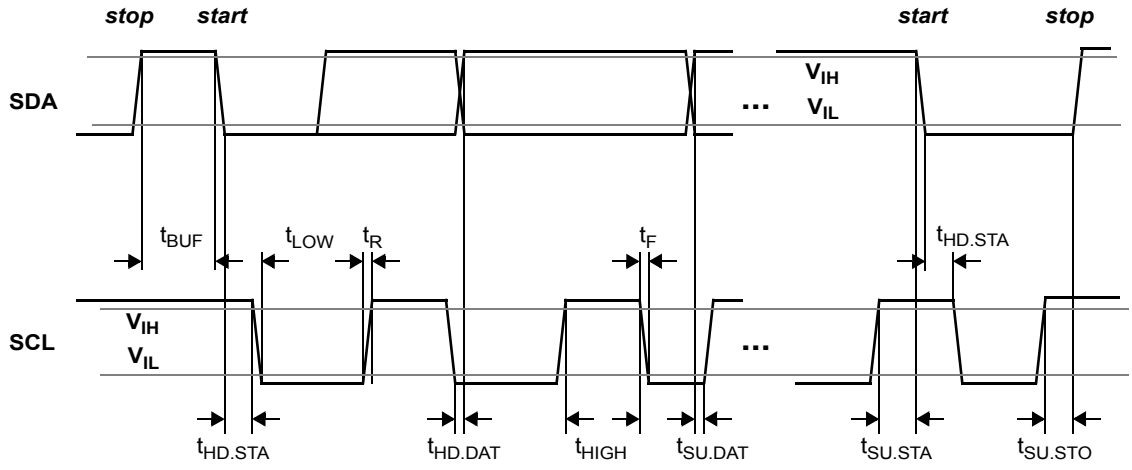
Table 7. **I²C interface - timing characteristics for Fast mode plus (1 MHz)**

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	—	1000	kHz
t_{LOW}	Clock pulse width low	0.5	—	—	µs
t_{HIGH}	Clock pulse width high	0.26	—	—	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	0.5	—	—	µs
$t_{HD.STA}$	Start hold time	0.26	—	—	µs
$t_{SU.STA}$	Start setup time	0.26	—	—	µs
$t_{HD.DAT}$	Data in hold time	0	—	0.9	µs
$t_{SU.DAT}$	Data in setup time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	120	ns
t_F	SCL/SDA fall time	—	—	120	ns
$t_{SU.STO}$	Stop setup time	0.26	—	—	µs
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
Cin	Input capacitance (SCL)	—	—	4	pF
C_L	Load capacitance	—	140	550	pF

Table 8. I²C interface - timing characteristics for Fast mode (400 kHz)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	—	400	kHz
t_{LOW}	Clock pulse width low	1.3	—	—	µs
t_{HIGH}	Clock pulse width high	0.6	—	—	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	1.3	—	—	ms
$t_{HD.STA}$	Start hold time	0.26	—	—	µs
$t_{SU.STA}$	Start setup time	0.26	—	—	µs
$t_{HD.DAT}$	Data in hold time	0	—	0.9	µs
$t_{SU.DAT}$	Data in setup time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	120	ns
t_F	SCL/SDA fall time	—	—	120	ns
$t_{SU.STO}$	Stop setup time	0.6	—	—	µs
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
Cin	Input capacitance (SCL)	—	—	4	pF
C_L	Load capacitance	—	125	400	pF

Figure 16. I²C timing characteristics



4 Electrical characteristics

4.1 Absolute maximum ratings

Table 9. Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
AVDD, IOVDD	-0.5	—	3.6	V
SCL, SDA, LPn, INT and I2C_RST	-0.5	—	3.6	

Note: Stresses above those listed in Section 1 Product overview may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Recommended operating conditions

Table 10. Recommended operating conditions

Parameter		Min.	Typ.	Max.	Unit
AVDD supply(1)	2.8 V configuration	2.5	2.8	3.3	V
	3.3 V configuration	3.0	3.3	3.6	
IOVDD supply	1.8 V configuration	1.62	1.8	1.98	
	2.8 V configuration	2.5	2.8	3.3	
	3.3 V configuration	3.0	3.3	3.6	
Ambient temperature (normal operating)		-30	—	85	°C

1. *AVDD is independent of IOVDD*

4.3 Electrostatic discharge (ESD)

The VL53L5CX is compliant with ESD values presented in the table below.

Table 11. ESD performances

Parameter	Specification	Conditions
Human body model	JEDEC JS-001-2014	± 2 kV, 1500 Ohms, 100 pF
Charged device model	JEDEC JS-002-2014	± 500 V

4.4 Current consumption

The current consumption values are given in the table below.

- Typical values quoted are for nominal voltage, process, and temperature (23 °C).
- Maximum values are quoted for worst case conditions (process, voltage, and temperature) unless stated otherwise (70 °C).

Table 12. Current consumption

Device State	Average current consumption				Unit
	AVDD		IOVDD		
	Typ.	Max.	Typ.	Max.	
LP idle	45	300	0.1	1	µA
HP idle	1.3	1.6	2.8	35	mA
Active ranging(1)	45	50	50	80	mA

1. *Active ranging is when the device is actively ranging. The current consumption is not affected by 4x4 or 8x8 zone configuration*

IOVDD peak current will be the average value +10 mA.
AVDD peak current will be the average current +10 mA.

Table 13. Example of typical power consumption in Continuous mode

Parameter	2V8/1V8	2V8/2V8	3V3/3V3	Unit
Continuous mode (4x4 mode or 8x8 mode)	216	266	313	mW

Table 14. Example of typical power consumption in Autonomous mode

Parameter	2V8/1V8	2V8/2V8	3V3/3V3	Unit
4x4 mode - 1 Hz frame rate with 5 ms integration time	2.8	3.7	4.5	mW
4x4 mode - 5 Hz frame rate with 5 ms integration time	11	16	19	
4x4 mode - 10 Hz frame rate with 45 ms integration time	95	133	156	
8x8 mode - 1 Hz frame rate with 5 ms integration time	8	11	11	

4.5 Digital input and output

The following tables summarize the digital I/O electrical characteristics.

Table 15. INT, I2C_RST, LPn

Symbol	Parameter	IOVDD configuration	Min.	Max.	Unit
V_{IL}	Low level input voltage	1.8 V	-0.3	0.35* IOVDD	V
		2.8 V - 3.3 V			
V_{IH}	High level input voltage	1.8 V	0.65*IOVDD	2.28	
		2.8 V - 3.3 V		3.6	
V_{OL}	Low level output voltage (I_{OUT} = 4 mA)	1.8 V	—	0.4	
		2.8 V - 3.3 V			
V_{OH}	High level output voltage (I_{OUT} = 4 mA)	1.8 V	1.22	—	
		2.8 V - 3.3 V	2.1		

Table 16. I^2C interface (SDA/SCL)

Symbol	Parameter	IOVDD configuration	Min.	Max.	Unit
V_{IL}	Low level input voltage	1.8 V	-0.3	0.54	V
		2.8 V - 3.3 V		0.3*IOVDD	
V_{IH}	High level input voltage	1.8 V	1.13	2.28	
		2.8 V - 3.3 V		3.6	
V_{OL}	Low level output voltage (I_{out} = 4 mA)	1.8 V	—	0.4	
		2.8 V- 3.3 V			
$I_{IL/IH}$	Leakage from IOVDD supply		—	2.5	µA
	Leakage from IOVDD pad		—	1	

Note: I^2C pads use 1V8 switching thresholds for all IOVDD supplies

Note: A maximum load of 12 mA is assumed in the above table

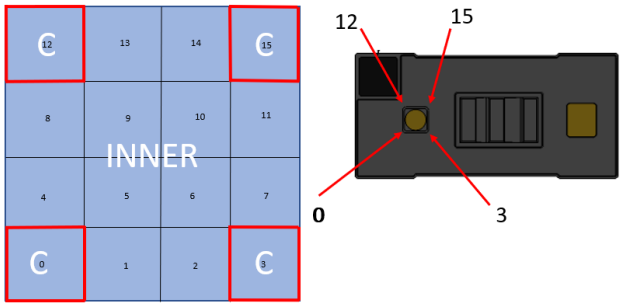
5 Ranging performance

5.1 Zone mapping

5.1.1 Zone mapping 4x4

The figure below shows the zone definition in 4x4 mode. There are 16 zones in total which increment along a row first before starting a new row. The physical view is from the device top into the lens. The numbers of each zone, as indicated in the figure below, corresponds to the ZoneIDs returned by the sensor.

Figure 17. Zone mapping in 4x4 mode

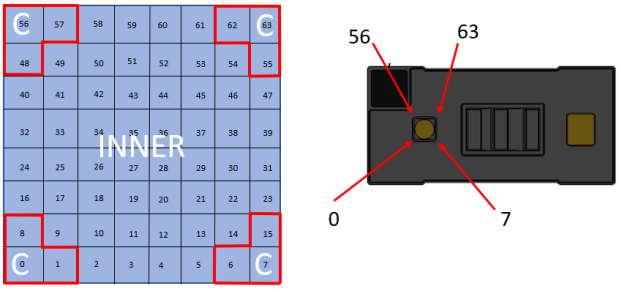


C = Corner zones
INNER = all zones not identified as the corner

5.1.2 Zone mapping 8x8

The figure below shows the zone definition in 8x8 mode. There are 64 zones in total which increment along a row first before starting a new row. The physical view is from the device top into the lens. The numbers of each zone, as indicated in the figure below, correspond to the ZoneIDs returned by the sensor to the host.

Figure 18. Zone mapping in 8x8 mode

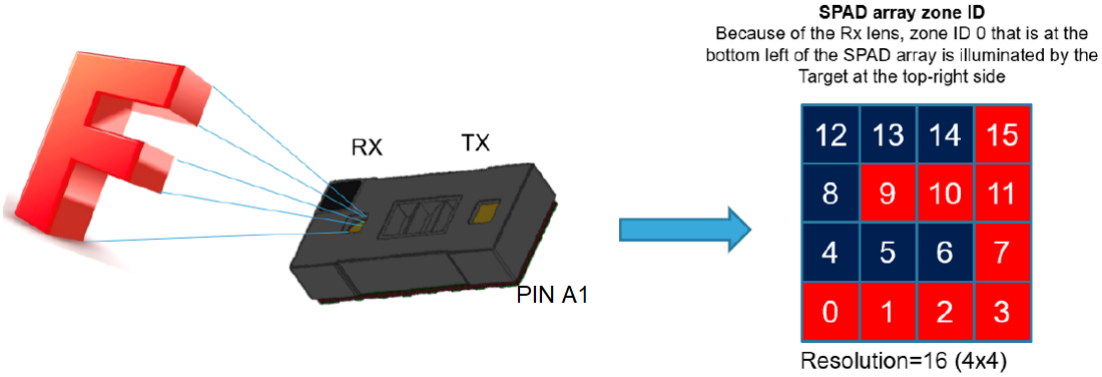


C = Corner zones
INNER = all zones not identified as the corner

5.1.3 Effective zone orientation

The VL53L5CX module includes a lens over the RX aperture which flips (horizontally and vertically) the captured image of the target. As a consequence, the zone identified as zone 0 in the bottom left of the SPAD array is illuminated by a target located at the top right hand side of the scene.

Figure 19. Effective orientation



5.2 Continuous ranging mode

5.2.1 Measurement conditions

The following criteria and test conditions apply to all the characterisation results detailed in this section unless specified otherwise:

- The specified target fills 100 % of the field of view of the device (in all zones).
- Targets used are Munsell N4.75 (17 %) and Munsell N9.5 (88 %).
- AVDD is 2.8 V, IOVDD is 1.8 V.
- Nominal ambient temperature is 23 °C.
- Maximum range capability is based on a 90 % detection rate (1).
- Range accuracy figures are based on 2.7 sigma ie 99.3 % of measurements are within the specified accuracy.
- Tests are performed in the dark and at 2 W/m^2 target illumination (940 nm). A 2 W/m^2 target irradiance at 940 nm is equivalent to 5 kLux daylight.
- All tests are performed without coverglass.
- The sensor relies on default calibration data.
- The device is controlled through the API using the default driver settings.

1. *Detection rate is a statistical value indicating the worst case percentage of measurements that return a valid ranging. For example, taking 1000 measurements with 90 % detection rate gives 900 valid distances. The 100 other distances may be outside the specification.*

5.2.2 Maximum ranging distance 4x4

The table below shows the maximum ranging capability of the VL53L5CX under different conditions. Refer to Section 5.2.1 Measurement conditions for the general test conditions.

Table 17. Maximum ranging capabilities when ranging continuously at 30 Hz

Target reflectance level. Full FoV (reflectance %)	Zone	Dark	Ambient light (5 klux)
White target (88 %)	Inner	Typical: 4000 mm Minimum: 4000 mm	Typical: 1700 mm Minimum: 1400 mm
	Corner	Typical: 4000 mm Minimum: 4000 mm	Typical: 1400 mm Minimum: 1100 mm
Grey target (17 %)	Inner	Typical: 2400 mm Minimum: 1900 mm	Typical: 1000 mm Minimum: 900 mm
	Corner	Typical: 2200 mm Minimum: 1800 mm	Typical: 950 mm Minimum: 850 mm

5.2.3 Maximum ranging distance 8x8

The table below shows the maximum ranging capability of the VL53L5CX under different conditions. Refer to Section 5.2.1 Measurement conditions for the general test conditions.

Table 18. Max ranging capabilities when ranging continuously at 15Hz

Target reflectance level. Full FoV (reflectance %)	Zone	Dark (0 klux)	Ambient light (5 klux)
White target (88 %)	Inner	Typical: 3500 mm Minimum: 2600 mm	Typical: 1100 mm Minimum: 950 mm
	Corner	Typical: 3100 mm Minimum: 1700 mm	Typical: 1000 mm Minimum: 800 mm
Grey target (17 %)(1)	Inner:	Typical: 1300 mm Minimum: 900 mm	Typical: 800 mm Minimum: 600 mm
	Corner	Typical: 1100 mm Minimum: 600 mm	Typical: 650 mm Minimum: 400 mm

1. *measured 13 % in IR at 940 nm*

5.2.4 Range accuracy - Continuous mode

The figure below illustrates how range accuracy is defined over distance.

Figure 20. Range accuracy vs distance

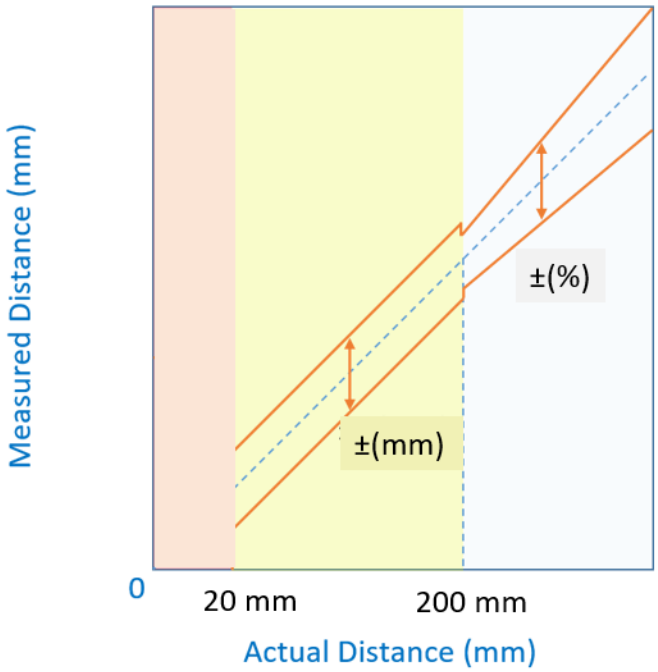


Table 19. Range accuracy

Distance	Mode	Target reflectance	Zones	Dark (0 klux)	Ambient light (5 klux)
20 - 200 mm	8x8 15Hz	Grey target (17 %)	All	±15 mm	15 mm
201 - 4000 mm	4x4 30Hz	White target (88 %)	All	±4 %	7%
		Grey target (17 %)		±5 %	8%
	8x8 15Hz	White target (88 %)		±5 %	8%
		Grey target (17 %)		±5 %	11%

5.3 Autonomous ranging mode

5.3.1 Measurement conditions

The following criteria and test conditions apply to all the characterisation results detailed in this section unless specified otherwise:

- The specified target fills 100 % of the field of view of the device (in all zones).
- Targets used are Munsell N4.75 (17 %) and Munsell N9.5 (88 %).
- AVDD is 2.8 V, IOVDD is 1.8 V.
- Nominal ambient temperature is 23 °C.
- Maximum range capability is based on a 90 % detection rate (1).
- Range accuracy figures are based on 2.7 sigma ie 99.3 % of measurements are within the specified accuracy.
- Tests are performed in the dark and at 2 W/m^2 target illumination (940 nm). A 2 W/m^2 target irradiance at 940 nm is equivalent to 5 kLux daylight.
- All tests are performed without coverglass.
- The sensor relies on default calibration data.
- The device is controlled thought the API using the default driver settings.

1. *Detection rate is a statistical value indicating the worst case percentage of measurements that return a valid ranging. For example, taking 1000 measurements with 90 % detection rate gives 900 valid distances. The 100 other distances may be outside the specification.*

5.3.2 Maximum ranging distance 4x4

Table 20. Maximum ranging capabilities when ranging with Autonomous mode at 30 Hz – 4x4 – integration time 5 ms

Target reflectance level. Full FoV (reflectance %)	Zone	Integration time (ms)	Dark (0 klux)	Ambient light (5 klux)
White target (88 %)	Inner	5	Typical : 3000 mm Minimum : 2700 mm	Typical : 1300 mm Minimum : 1100 mm
	Corner	5	Typical : 2700 mm Minimum : 2400 mm	Typical : 1200 mm Minimum : 1000 mm
Grey target (17 %)	Inner	5	Typical : 1100 mm Minimum : 900 mm	Typical : 800 mm Minimum : 600 mm
	Corner	5	Typical : 1000 mm Minimum : 800 mm	Typical : 700 mm Minimum : 500 mm

Table 21. Maximum ranging capabilities when ranging with Autonomous mode at 15 Hz – 8x8 – integration time 5 ms

Target reflectance level. Full FoV (reflectance %)	Zone	Integration time (ms)	Dark (0 klux)	Ambient light (5 klux)
White target (88 %)	Inner	5	Typical : 1900 mm Minimum : 1700 mm	Typical : 900 mm Minimum : 800 mm
	Corner	5	Typical : 1600 mm Minimum : 1300 mm	Typical : 800 mm Minimum : 650 mm
Grey target (17 %)	Inner	5	Typical : 800 mm Minimum : 600 mm	Typical : 500 mm Minimum : 400 mm
	Corner	5	Typical : 600 mm Minimum : 500 mm	Typical : 400 mm Minimum : 300 mm

5.3.3 Range accuracy - Autonomous mode

Table 22. Range accuracy – Autonomous mode

Distance (mm)	Mode	Integration time (ms)	Reflectance	Dark (0 klux)	Ambient light (5 klux)
20-200 mm	8x8 15 Hz	5 ms	White 88 %	±17 mm	±20 mm
201-4000mm	4x4 30 Hz	5 ms	Grey 17 %	±6 %	±10 %
		5 ms	White 88 %	±5 %	±8 %
	8x8 15 Hz	5 ms	Grey 17 %	±8 %	±12 %
		5 ms	White 88 %	±7 %	±10 %

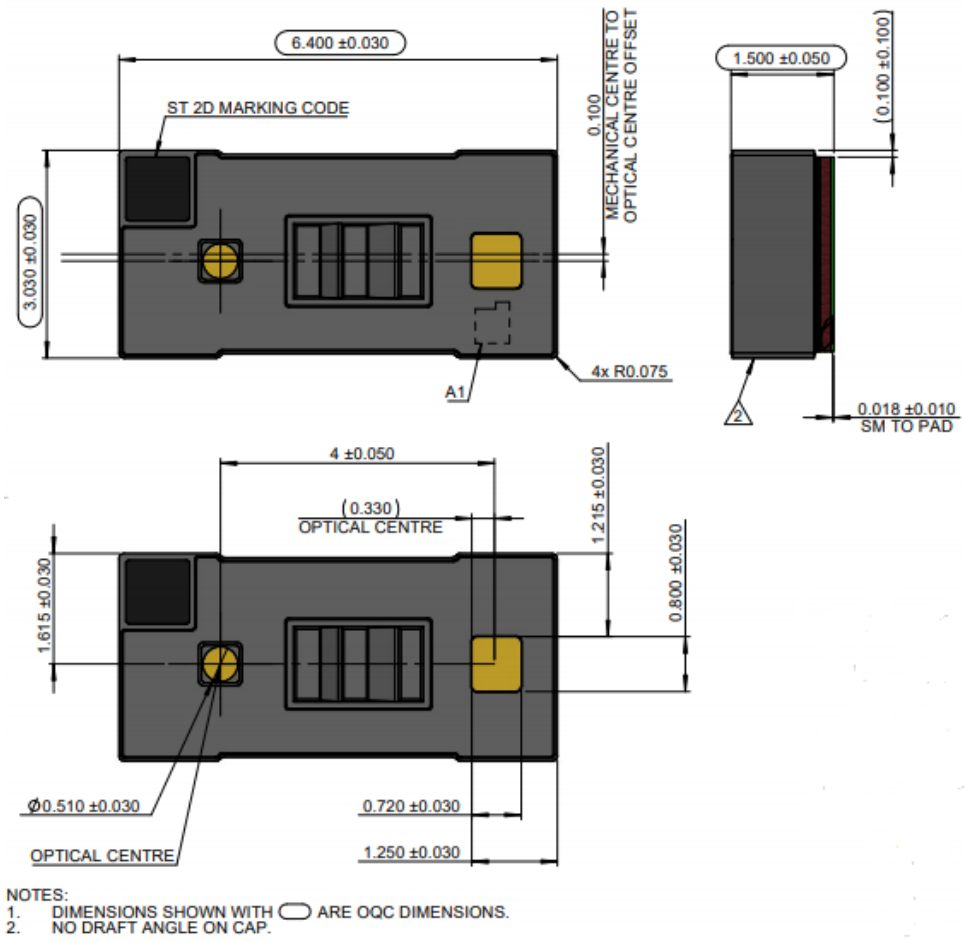
5.4 Range offset drift over temperature

Any increase in silicon temperature either from selfheating or a change in ambient temperature results in a range offset drift which may be minimised by performing periodic autocalibration, resulting in typical drift of 0.05 mm/°C.

6 Outline drawings

The figures below gives details of the VL53L5CX module.

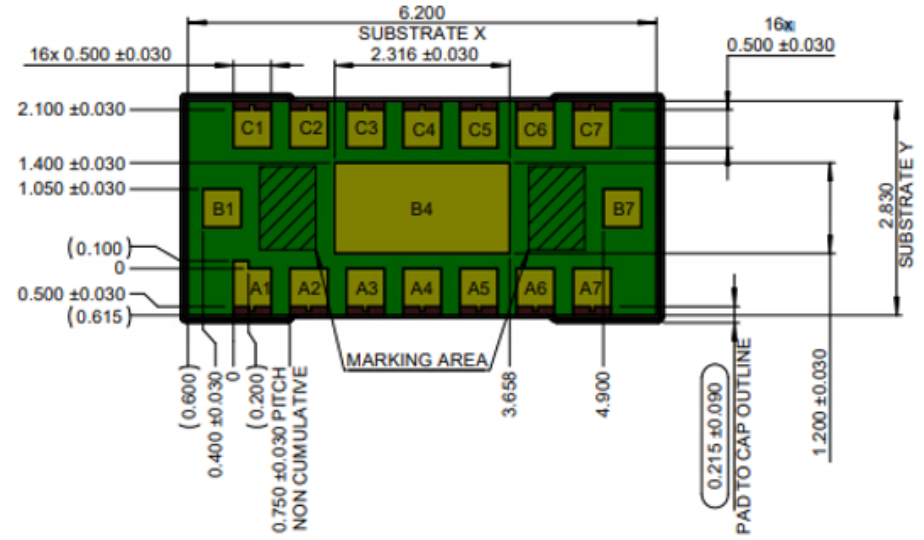
Figure 21. Outline drawing (page 1/4)



Note: SM stands for solder mask.

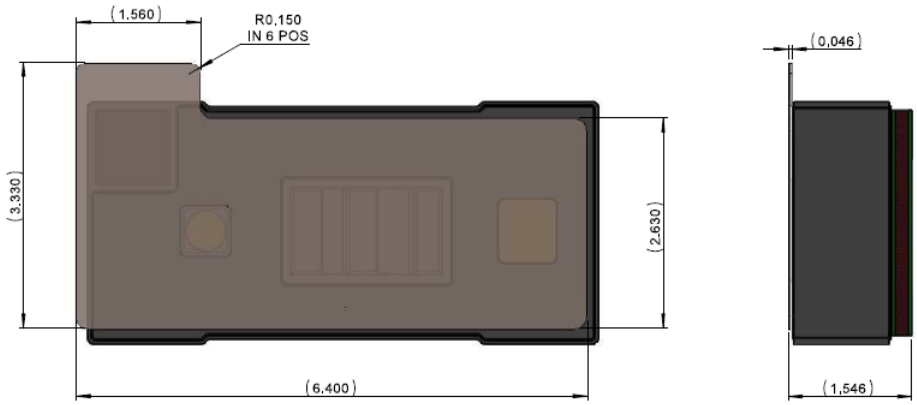
Note: A thermal pad is required on the application board for thermal dissipation purpose. For more information, refer to AN5657.

Figure 22. **Outline drawing (page 2/4)**



Note: For more information, refer to the pin description in Table 3. VL53L5CX pin description.

Figure 23. **Outline drawing (page 3/4) - Module with liner**



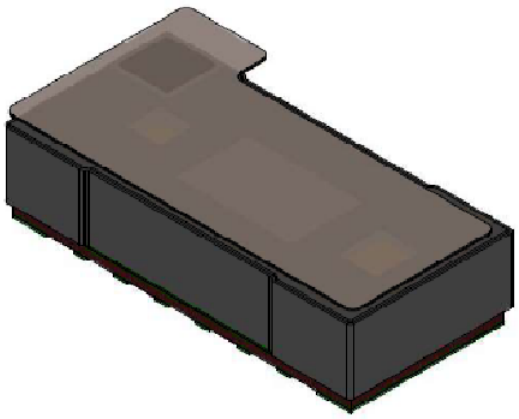
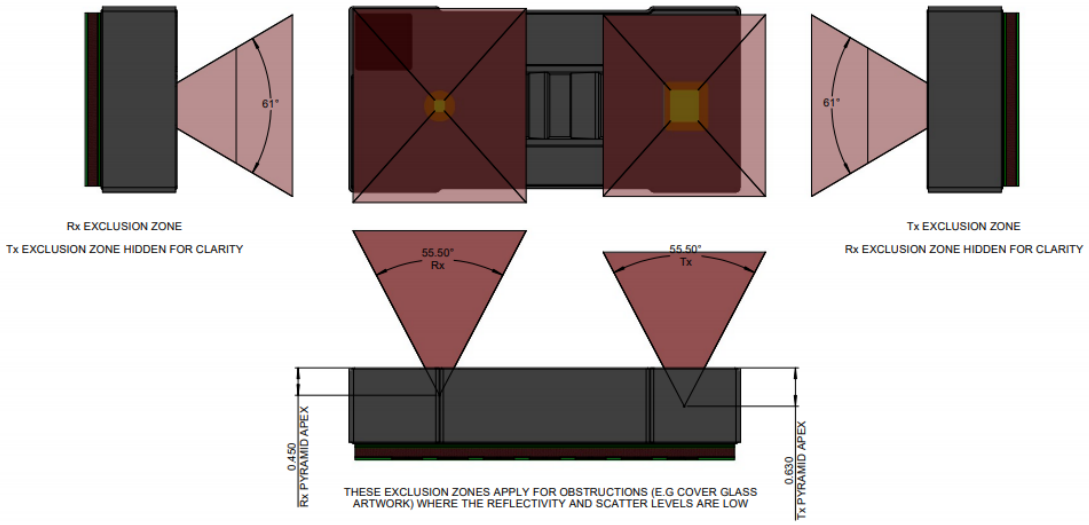


Figure 24. Outline drawing (page 4/4)



7 Laser safety considerations

The laser output power must not be increased by any means and no optics should be used with the intention of focusing the laser beam.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Figure 25. Class 1 laser label

Figure 26. Laser notice 50: applies to IEC 60825-1:2007

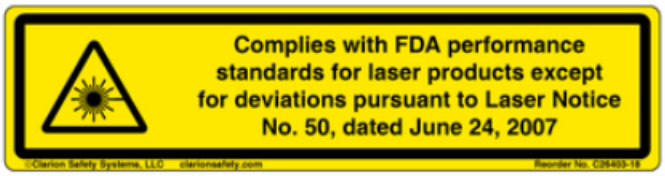
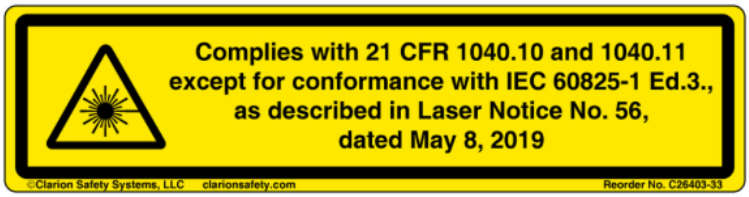


Figure 27. Laser notice 56: applies to IEC 60825-1:2014

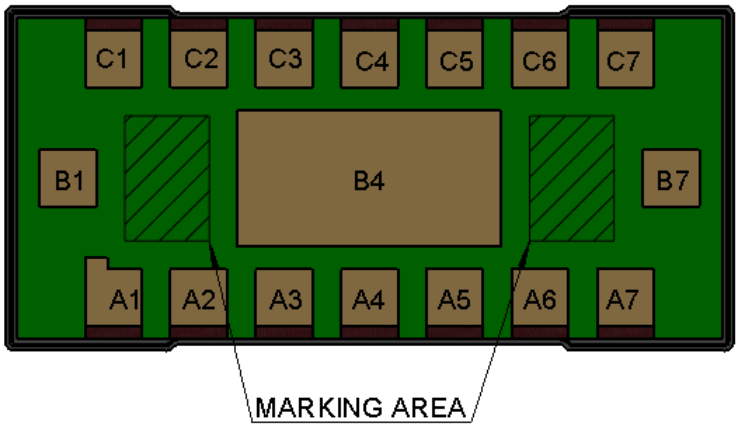


8 Packaging and labeling

8.1 Product marking

See the figure below for the product marking area. The marking is L5C-

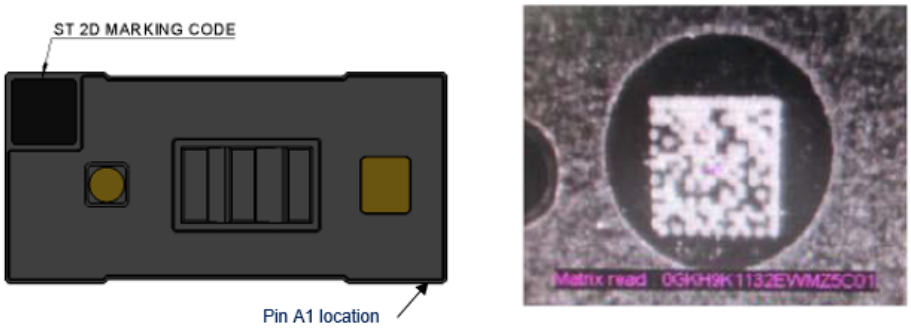
Figure 28. Product marking area



A 2D product marking code is applied on the corner of the module cap as shown in the figure below.

Note: The 2D marking code aligns with pin C7 of the module and is not an indicator of pin 1.

Figure 29. 2D product marking code



8.2 Inner box labeling

The labeling follows the ST standard packing acceptance specification.

The following information is on the inner box label:

- Assembly site
- Sales type
- Quantity
- Trace code
- Marking
- Bulk ID number

8.3 Packing

At customer/subcontractor level, it is recommended to mount the VL53L5CX in a clean environment.

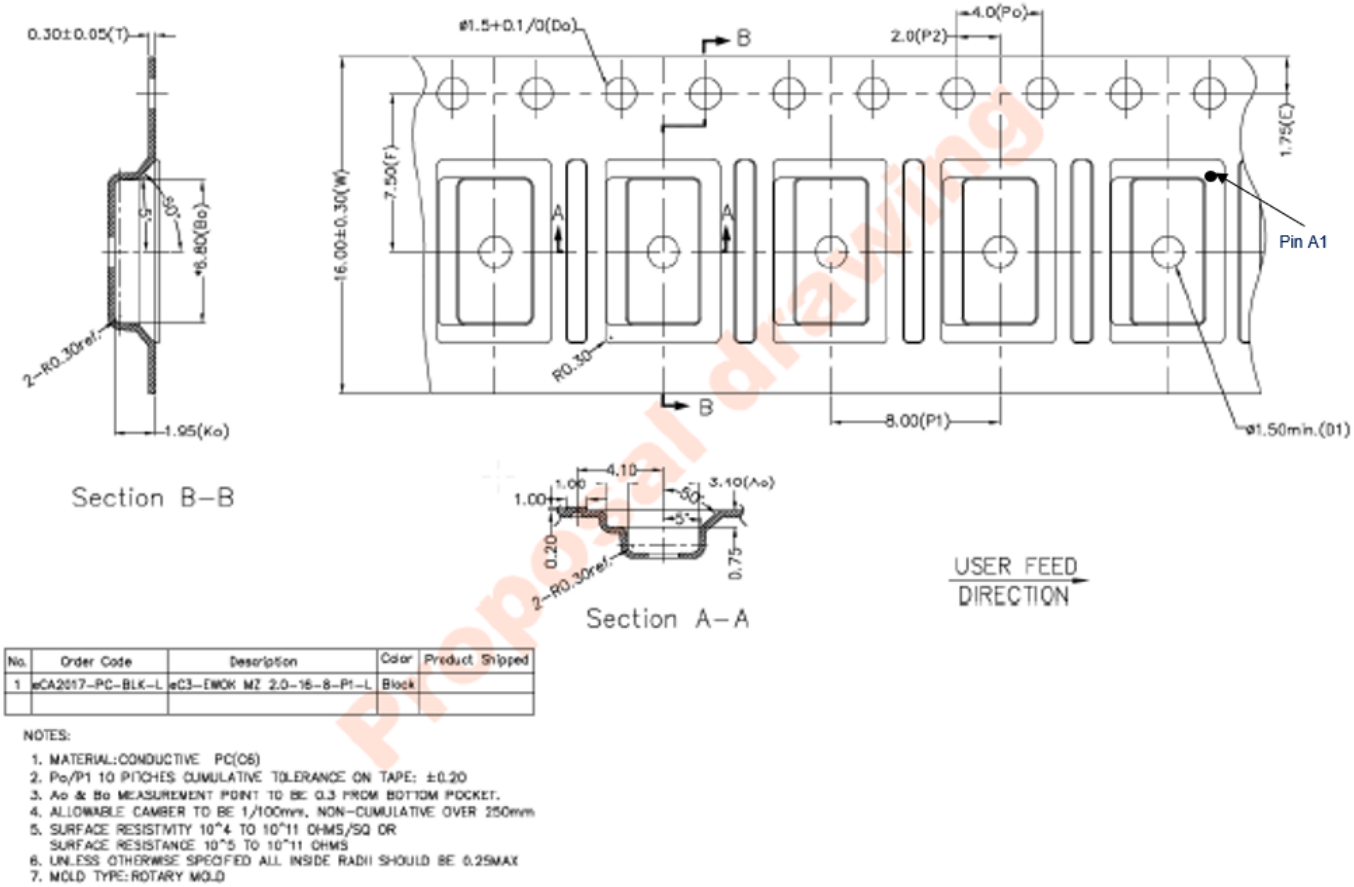
To help avoid any foreign material contamination at final assembly level the modules are shipped in a tape and reel format with a protective liner.

The liner is compliant with reflow at 260 °C (as per JEDEC-STD-020E).

Note: The liner must be removed during assembly of the customer device, just before mounting the cover glass.

8.4 Tape outline drawing

Figure 30. VL53L5CX tape outline and reel packaging drawing



No.	Order Code	Description	Color	Product Shipped
1	eCA2017-PC-BLK-L	eC3-EWOK MZ 2.0-16-8-Pt-L	Black	

NOTES:

1. MATERIAL:CONDUCTIVE PC(C6)
2. Po/P1 10 PITCHES CUMULATIVE TOLERANCE ON TAPE: ±0.20
3. Ao & Bo MEASUREMENT POINT TO BE 0.3 FROM BOTTOM POCKET.
4. ALLOWABLE CAMBER TO BE 1/100mm, NON-CUMULATIVE OVER 250mm
5. SURFACE RESISTIVITY 10^4 TO 10^11 OHMS/SQ OR
   SURFACE RESISTANCE 10^5 TO 10^11 OHMS
6. UNLESS OTHERWISE SPECIFIED ALL INSIDE RADII SHOULD BE 0.25MAX
7. MOLD TYPE:ROTARY MOLD

8.5 Pb-free solder reflow process

The table and figure below show the recommended and maximum values for the solder profile.

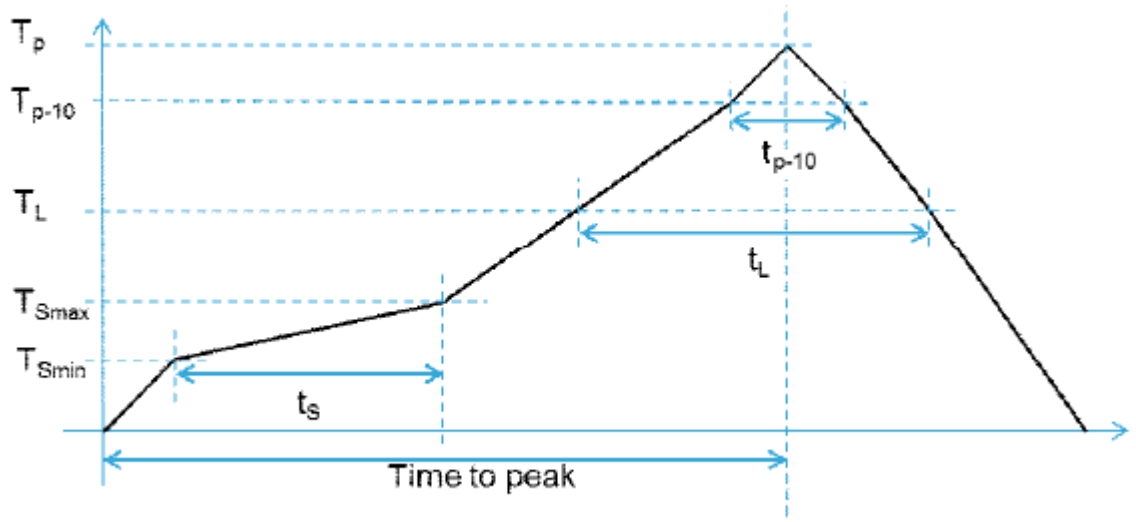
Customers have to tune the reflow profile depending on the PCB, solder paste and material used. We expect customers to follow the “recommended” reflow profile, which is specifically tuned for the VL53L5CX package.

For any reason, if a customer must perform a reflow profile which is different from the “recommended” one (especially peak >240 °C), the new profile must be qualified by the customer at their own risk. In any case, the profile has to be within the “maximum” profile limit described in the table below.

Table 23. Recommended solder profile

Parameters	Recommended	Maximum	Units
Minimum temperature (T_S min)	130	150	°C
Maximum temperature (T_S max)	200	200	°C
Time t_s (T_S min to T_S max)	90-110	60-120	s
Temperature (T_L)	217	217	°C
Time (t_L)	55-65	55-65	s
Ramp up	2	3	°C/s
Temperature (T_{p-10})	—	235	°C
Time (t_{p-10})	—	10	s
Ramp up	—	3	°C/s
Peak temperature (T_p)	240	260	°C
Time to peak	300	300	s
Ramp down (peak to T_L)	-4	-6	°C/s

Figure 31. Solder profile



Note: The component should be limited to a maximum of three passes through this solder profile.

Note: As the VL53L5CX package is not sealed, only a dry reflow process should be used (such as convection reflow). Vapor phase reflow is not suitable for this type of optical component.

Note: The VL53L5CX is an optical component and as such, it should be treated carefully. This would typically include using a ‘no-wash’ assembly process.

8.6 Handling and storage precautions

8.6.1 Shock precautions

Sensor modules house numerous internal components that are susceptible to shock damage. If a unit is subject to excessive shock, is dropped on the floor, or a tray/reel of units is dropped on the floor, it must be rejected, even if no apparent damage is visible.

8.6.2 Part handling

Handling must be done with non-marring ESD safe carbon, plastic, or teflon tweezers. Ranging modules are susceptible to damage or contamination. The customer is advised to use a clean assembly process until a protective cover glass is mounted.

8.6.3 Compression force

A maximum compressive load of 25 N should be applied on the module.

8.6.4 Moisture sensitivity level

Moisture sensitivity is level 3 (MSL) as described in IPC/JEDEC JSTD-020-C.

Note: If devices are stored out of the packaging for more than 168 hours, the devices should be baked before use. The optimum bake recommended is at + 90 °C for a minimum of 6 hours.

8.7 Storage temperature conditions

Table 24. Recommended storage conditions

Parameter	Min.	Typ.	Max.	Unit
Temperature (storage)	-40	23	90	°C

9 Ordering information

The VL53L5CX is currently available in the formats below. More detailed information is available on request.

Table 25. Order codes

Order codes	Package	Packing	Minimum order quantity
VL53L5CXV0GC/1	Optical LGA16 with liner	Tape and reel	3600 pcs

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11 Acronyms and abbreviations

Acronym/abbreviation	Definition
AF	autofocus
API	application programming interface
AR/VR	augmented reality/virtual reality
DOE	diffractive optical element
ESD	electrostatic discharge
FoV	field of view
FoI	field of illumination
GPIO	general purpose input output
HP	high power
I^2C	inter-integrated circuit (serial bus)
LAF	laser autofocus
LGA	land grid array
LP	low power
NVM	non-volatile memory
PCB	printed circuit board
PDAF	phase detection autofocus
PLL	phase-locked loop
PVT	process, voltage and temperature
POR	power on reset
RAM	random-access memory
SPAD	single photon avalanche diode
SW	software
ToF	Time-of-Flight
UI	user interface
UM	user manual
VCSEL	vertical cavity surface emitting laser

Revision history

Table 26. **Document revision history**

Date	Version	Changes
06-Jul-2021	1	Initial release

Contents

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