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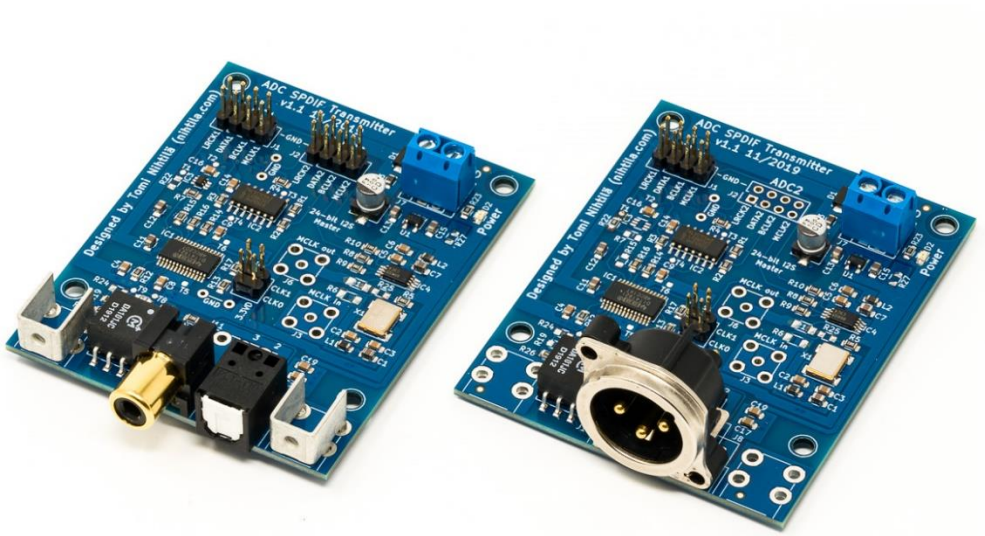
SPDIF TX

I2S to S/PDIF converter



FEATURES

- I2S input
- Sample rate 48 / 96 / 192 kHz
  - Selectable by jumper link
- Various S/PDIF output options
  - Galvanic isolation
- Onboard 24.576 MHz oscillator or external MCLK
- Single 5 V supply

INPUTS

- I2S input, SPDIF TX is Master
  - LRCK – Word clock (output)
  - BCLK – Bit clock (output)
  - DATA – Audio data (input)
- Stereo I2S or Dual Mono (supports 2x ADC AK5572 in mono mode)
- Signal level is 3.3 V

OUTPUTS

- Two S/PDIF output options
  - Coax (RCA) and Optical (Toslink)
  - AES/EBU (XLR)
- All outputs are galvanically isolated

APPLICATIONS

- S/PDIF output for AD-converter
  - Specifically designed for ADC AK5572, supporting dual mono mode
- S/PDIF output for any Slave I2S source

SPDIF TX is an I2S to S/PDIF digital audio converter. It takes in I2S serial audio data in either conventional stereo format or specific dual mono format used in nihtila.com ADC AK5572 AD-converter.

In dual mono mode SPDIX TX takes in two stereo (in ADC AK5572 dual mono mode both channels have identical data) streams and picks one channel from stream 1 and the other channel from stream 2.

S/PDIF output is always normal stereo stream.

Sample rate is selected with two jumper links and can be 48 kHz, 96 kHz, or 192 kHz. It is the same for both I2S input and S/PDIF output.

The board uses 24.576 MHz Master Clock which can be taken from an onboard crystal oscillator or provided externally using an optional SMB connector and termination resistor. MCLK is then split into four using a dedicated clock splitter IC. One spare clock output is available on optional SMB connector to use elsewhere in the system.

Two output options are available:

- Coax (RCA) and Optical (Toslink)
- AES/EBU (XLR)

In addition, input can be configured for stereo I2S or dual mono I2S, effectively meaning four variants of the board. All use the same PCB though.

Note that photo above shows two different board options. One SPDIF TX contains only one board.

HARDWARE DETAILS

- DIT4192 digital audio transmitter
- CDCLVC1104 clock splitter
- Transformer for S/PDIF isolation
- SMB and 50 Ω termination option for Master Clock input
- SMB for extra Master Clock output

SYSTEM REQUIREMENTS

- 5 V digital supply, 35 mA
- 24.576 MHz MCLK if onboard oscillator is not used
- Source must be I2S Slave
- 3.3 V signal level

INFORMATION AND CONTACT

- http://nihtila.com for general up to date information and shop
- Youtube for videos
- Follow Twitter (@nihtilacom)
- Contact (http://nihtila.com/contact/)

DOCUMENT VERSION

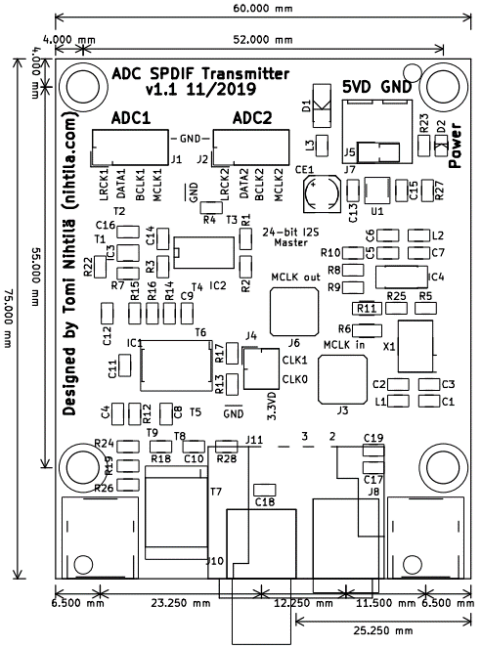
v1.1.0 (01/2020) for SPDIF TX v1.1

Configuration and settings

Sample rate is the only needed setting in SPDIF TX. Everything else is handled automatically by the circuit.

Sample rate is selected with two jumper links in pinheader J4; see table below. In fact, these jumpers select MCLK/fs ratio, and by using 24.576 MHz MCLK the values in the table can be chosen.

Configuration between stereo or dual mono input and which output connector to use are done by component selection. These can be selected when buying or building a board.



Sample rate selection with jumper links J4. Sample rate fs depends on Master Clock; MCLK is integer multiple of fs. Values are given for 24.576 MHz MCLK.

CLK1	CLK0	Sample rate
open	open	192 kHz (128x fs)
open	close	96 kHz (256x fs)
close	*open*	*64 kHz (384x fs)*
close	close	48 kHz (512x fs)