tynemouth software

TYNEMOUTH SOFTWARE MINSTREL ISSUE THREE

PARTS LIST

CAPACITORS – AXIAL CERAMIC RATED 16V OR HIGHER

4 x 47pF *(usually marked 47 or 470)*
2 x 47nF *(usually marked 47n or 473)*
19 x 100nF *(usually marked 100n or 104)*
1 x 1uF *(usually marked 1u or 105)*
1 x 22µF *(axial electrolytic rated 25V)*

RESISTORS – ALL ¼W 5% OR BETTER (4 BAND RESISTOR COLOUR CODES SHOWN)

2 x 75Ω
1 x 180Ω
1 x 330Ω
1 x 470Ω
2 x 680Ω
12 x 1KΩ
3 x 2.2KΩ
1 x 4.7KΩ
7 x 10KΩ
1 x 220KΩ
1 x 1MΩ

(fit in positions marked 10K and 47K)

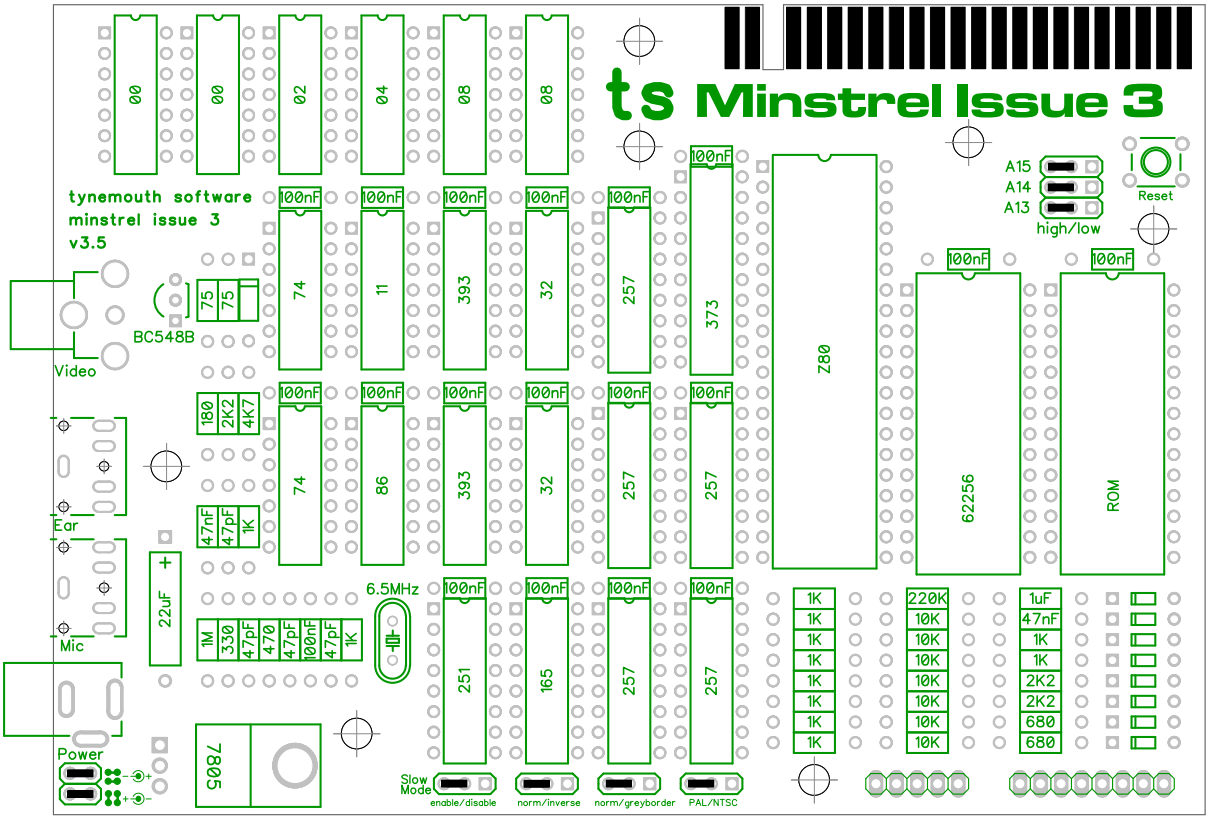
SEMICONDUCTORS - NEW TEXAS INSTRUMENTS 74HC SERIES CHIPS RECOMMENDED. 74LS SERIES CAN ALSO BE USED, BUT DO NOT MIX TYPES, ALL 74HC OR ALL 74LS.

9 x 1N4148 diode
1 x BC548B or similar NPN transistor
2 x 74HC00
1 x 74HC02
1 x 74HC04
2 x 74HC08
1 x 74HC11
2 x 74HC32
2 x 74HC74
1 x 74HC86
1 x 74HC165
1 x 74HC251
5 x 74HC257
1 x 74HC373
2 x 74HC393
1 x Z80 CPU / NEC D780 / Zilog Z84C0006PEG / Z84C0008PEG / Z84C0010PEG (4MHz or higher rated)
1 x 7805 or 7805 switching replacement (rated at least 250mA, more if using expansion port)
1 x 27C64 – 27C512 EPROM
1 x 62256 32K SRAM 600mil wide (e.g. Alliance AS6C62256 or Cyprus CY62256)
1 x 6.5 MHz Crystal (HC-49/U package)

CONNECTORS / SWITCHES

1 x 5 way, 1 x 8 way 0.1" FFC connector (for ZX81 membrane) *(e.g. TE Connectivity 5-520315-5, 5-520315-8)* or to suit keyboard
2 x Stereo 3.5mm Jack *(e.g. CUI SJ1-3525N – Digi-Key SJ1-3525N)*
1 x Phono jack *(e.g. CUI RCJ-011 – Digi-Key CP-1400-ND)*
1 x 2.1 mm DC Jack
1 x miniature tactile switch 6x6mm *(optional, e.g. Diptronics DTS-61N)*
2 x 2 way and 7 x 3 way headers with jumper *(optional or wire links)*
2 x 28pin, 1 x 40pin IC sockets *(turned pin recommended)*
14 x 14pin, 7 x 16pin, 1 x 20pin IC sockets *(optional, turned pin recommended)*

COMPONENT PLACEMENT



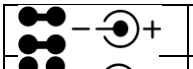
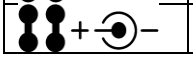
Note on the first run of boards, there are six resistors marked 47K, and one 10K, the design has been revised and 10K should be fitted for all seven of those parts, as shown above.

JUMPERS

Jumpers or link wires need to be fitted to the positions marked with black lines above; these are shown in the default configuration of centre negative supply, normal PAL video, top ROM address, no border and NMI slow mode enabled.

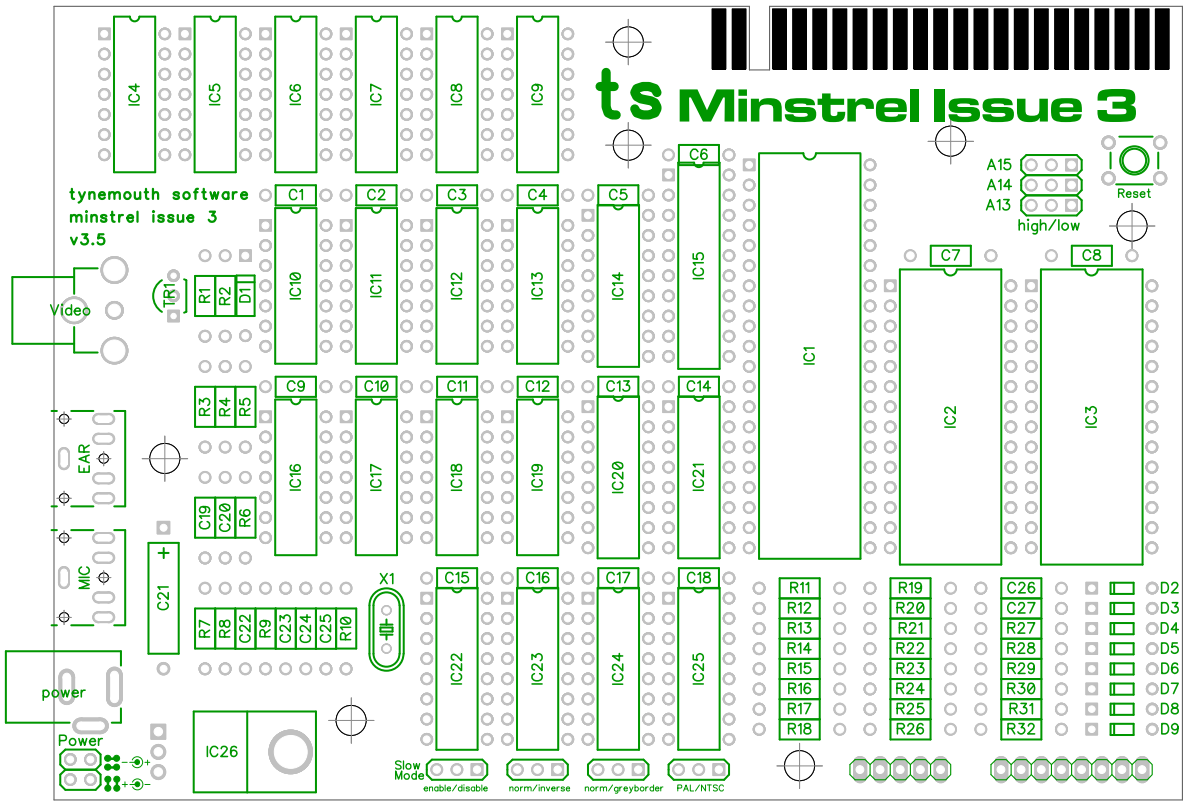
Jumper	●●□	○●■
Slow Mode	ZX81 style Fast / Slow mode	ZX80 style permanent Fast mode
Normal / Inverse	Normal (black on white) video	Inverse (white on black) video
Normal / Greyborder	Normal, border same as background	Grey crosshatch border
PAL / NTSC	PAL 50 Hz refresh rate	NTSC 60 Hz refresh rate
A15	High (5V) on ROM pin 1	Low (0V) on ROM pin 1
A14	High (5V) on ROM pin 27	Low (0V) on ROM pin 27
A13	High (5V) on ROM pin 26	Low (0V) on ROM pin 26

The jumpers near the power connector set the polarity of the power input

	Centre negative, used by optional TFW8b.com supply (also Spectrum and Commodore 16 computers)
	Centre positive, used by pretty much every other power supply

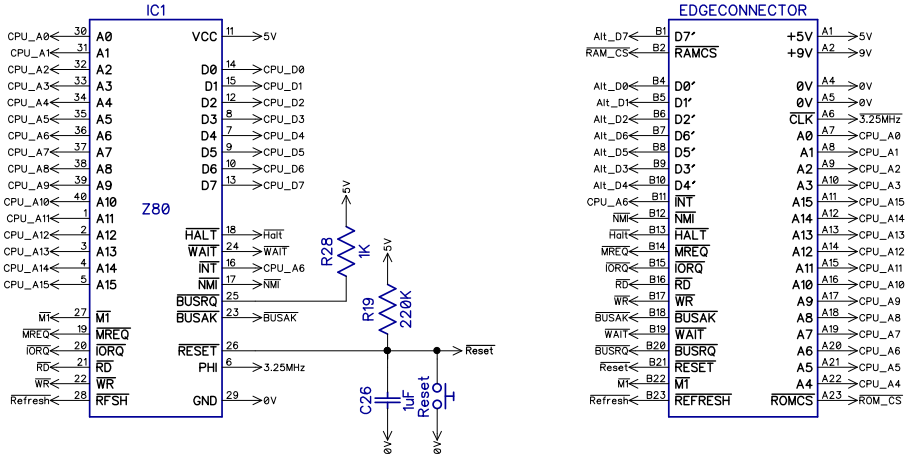
Power requirements are 9V DC. Current consumption is around 60mA for the board alone using HC chips, 200mA using LS chips. More if you plan to use the expansion port.

COMPONENT DESIGNATORS



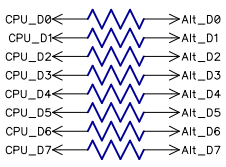
SCHEMATIC

The Schematic has been split into parts for clarity. The first is the Z80 and expansion connector. A simple RC circuit provides a reset pulse. BUSRQ is the only input not used, so that is tied high. Note A6 is connected directly to the IRQ pin. Likewise NMI and HALT are driven direct so these are not suitable for external inputs.



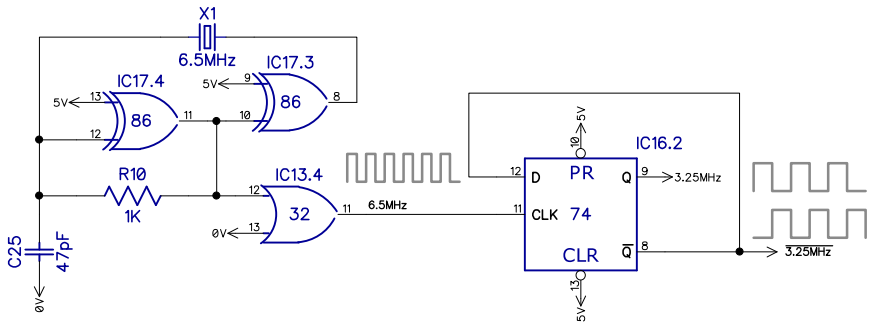
The databus is split as part of the display generation circuitry, using eight 1K resistors. The alternate databus is fed to the expansion connector. This allows the Z80 to see NOP operations and clock through the address space whilst the display circuitry is processing character data.

R11-18 8x 1K

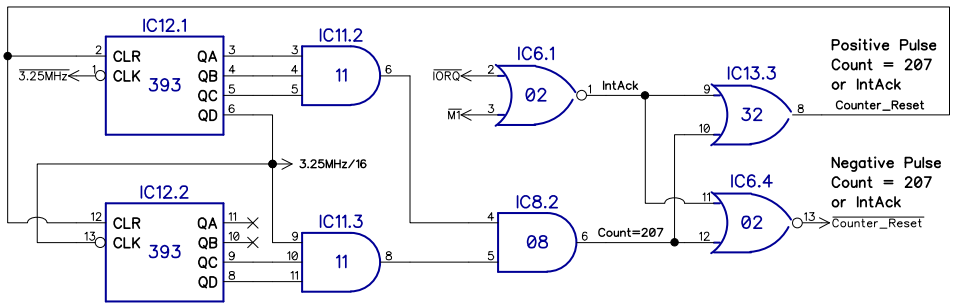


TIMING

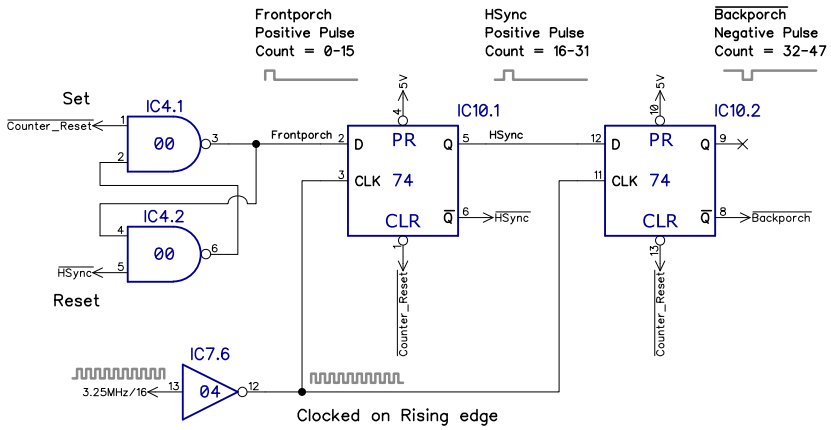
The main clock is 6.5MHz, which is divided down to 3.25MHz for the CPU.



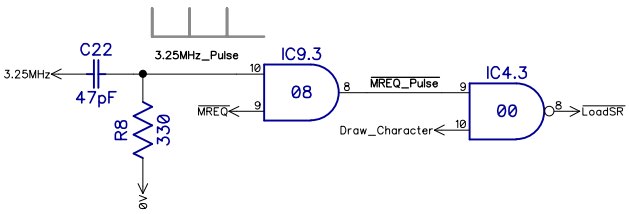
Two cascaded 4 bit counters run from the 3.25MHz clock, resetting every 207 cycles, a frequency of 15.7KHz. The counter is also reset by the IntAck condition when the Z80 is acknowledging the interrupt generated at the end of each display line.



When the counter is reset, it sets the flip flop which generates a frontporch signal. This is not used in the video generation, but is clocked through two D type flip flops to generate a single HSync pulse and then a single backporch pulse each cycle. The output of the first D type flip flop resets the frontporch flip flop to prevent further pulses during the cycle. The D types are clocked every 16 cycles (a frequency of 203.125KHz), giving pulses which are 4.92uS, close enough to the composite video requirements of 4.7uS for the HSync and 5.8uS for the backporch.

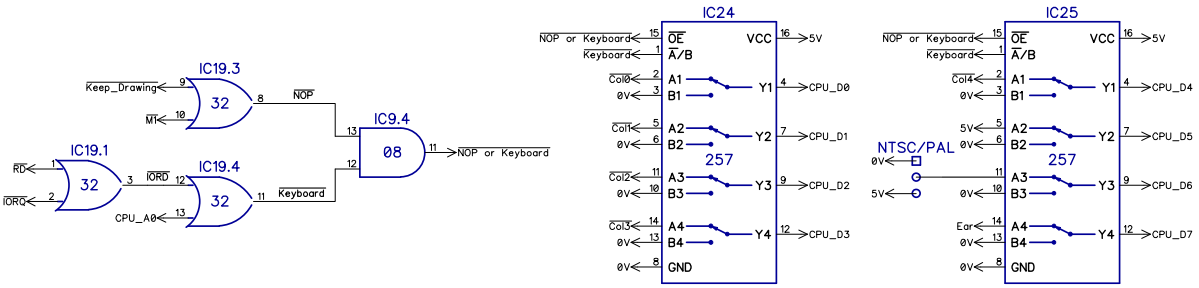


The shift register is loaded at the start of the T1 cycle, when the clock pulse is high and this is not a memory request.

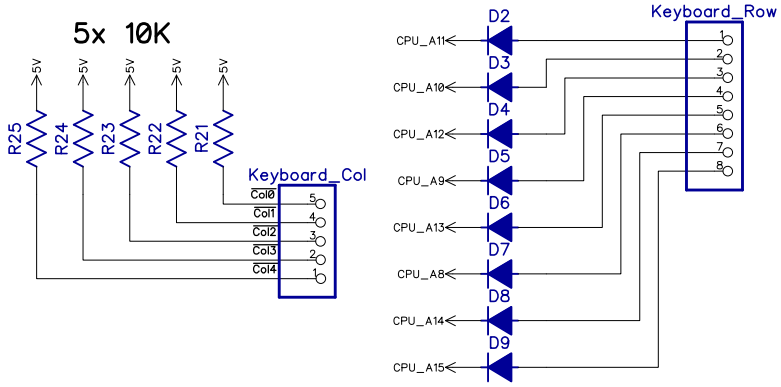


INPUT PORT

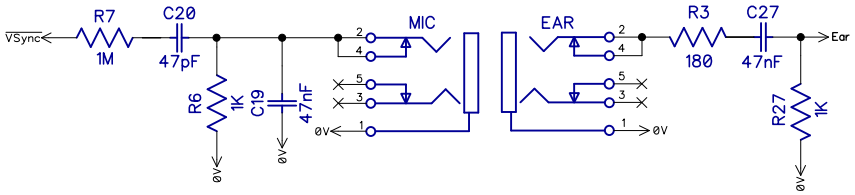
The IO decoding is fairly minimal. There is a single input port which is decoded only with A0, so it can be read on any address where A0 is low, all even numbered addresses. The input port is implemented using two multiplexor chips. These are shared with the NOP generator as both need to write to the CPU data lines. If a NOP is required, all the lines are connected to 0V which generates the opcode for NOP. If the keyboard is being read, the databus is connected to the input port. When neither are in use, the output of the multiplexor chips are set to high impedence.



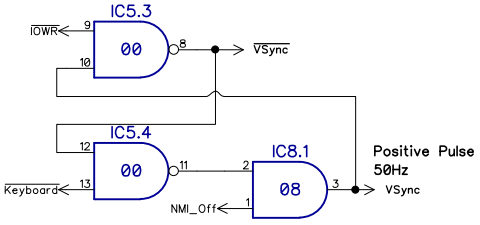
The keyboard is read using bits 0-4 of the input port. There are five column lines, which are pulled high normally. When the keyboard is being scanned, the upper eight address lines are set so that one is low at a time. If a key is pressed on the 5x8 crosspoint keyboard on that row, the column line reads low.



Bit 5 of the input port is not used, it will always read as a 1.
Bit 6 of the input port is used for PAL/NTSC selection, low for NTSC, high for PAL.
Bit 7 of the input port is used for cassette input. Data storage uses a cassette recorder (or these days a smart phone app). The cassette output uses the output of the VSync flip flop. This does not contain any horizontal sync pulses, so is cleaner than the original design which used the composite sync.

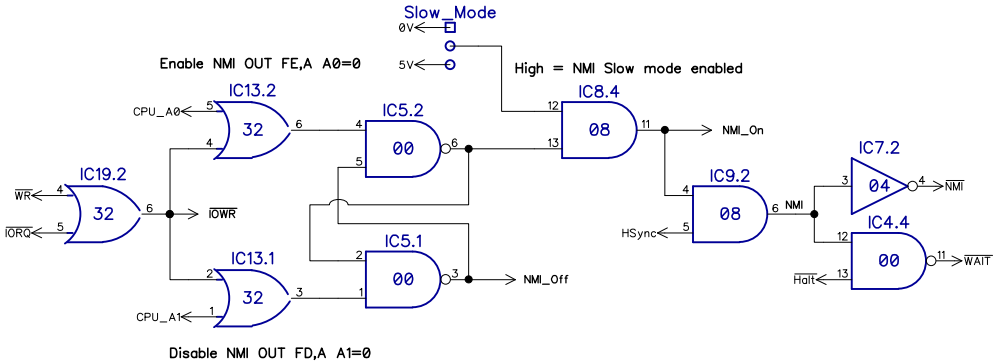


When a read operation to the keyboard port occurs, this sets the VSync flip flop to generate the VSync pulse. Any IO write operation clears it again. When NMI mode is active, this mechanism is disabled to avoid unwanted sync pulses.



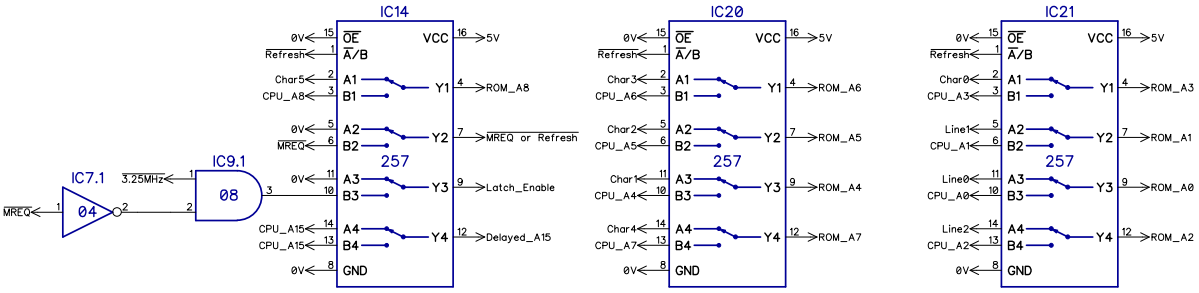
OUTPUT PORTS

Ports 0xFE and 0xFD are used to control the slow mode. Writing to port 0xFE activates slow mode, writing to port 0xFD disables it again. If the jumper is set high this will create a NMI pulse when there is an HSync pulse. There is some additional logic which ensures the CPU is in the correct T state, WAIT will be pulled low (active) when HALT is high (inactive) and NMI is low (active).

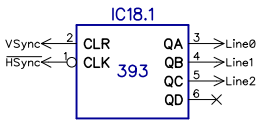


ADDRESS MULTIPLEXING

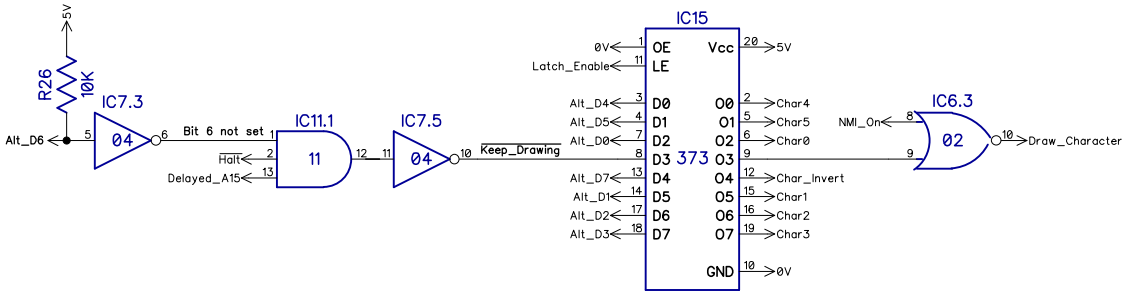
The ROM address during normal read operations is switched to the CPU address bus, but during display generation, the address is composed of multiple parts. A spare gate on the multiplexor is used to form a logic gate to generate a signal when MREQ is low or Refresh is low. A second spare gate is used to delay the A15 line slightly to avoid a timing glitch.



The lower three bits are generated from a line counter, this counts up each line, and is reset on a vertical sync so it is always on line 0 at the start.

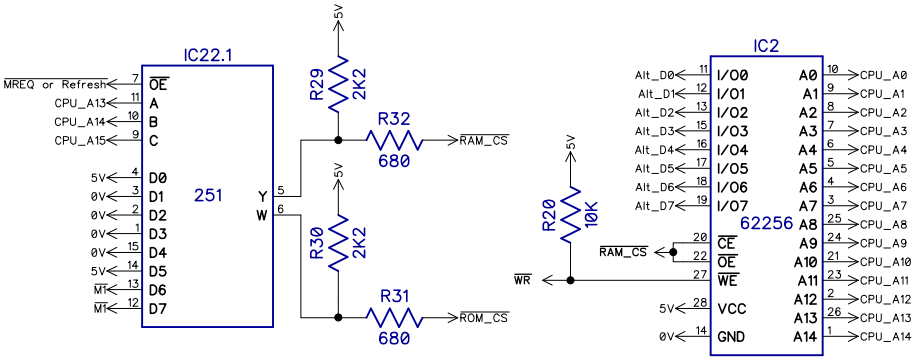


Bits 3-8 are set based on the character currently being displayed, which is latched when data is valid at the start of the next cycle. The last gate of the multiplexor is again used as a logic gate to generate the latch signal when refresh is low, the clock is low and MREQ is high.

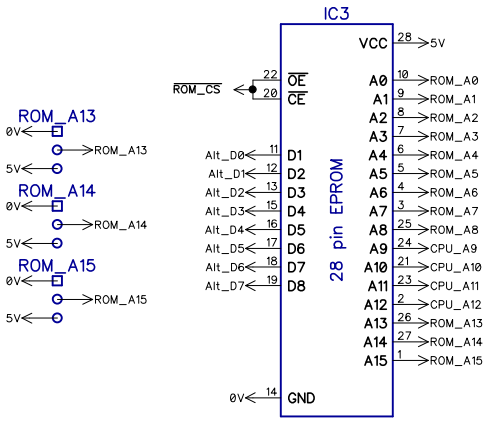


RAM AND ROM

The address decoding use an 8 input multiplexor, controlled by the upper three address lines. This selects the RAM_CS for the address range split into eight 8K blocks. When the selected input is low, the RAM is enabled, and when high, the ROM is enabled. The 2K2 resistors hold both ROM and RAM disabled when not in a memory request or refresh cycle (i.e. the screen is being drawn). The 680Ω resistors allow the RAM_CS and ROM_CS lines to be overridden from the expansion port. The 10K resistor holds the RAM write line high, to put the chip in read mode when not being driven by the CPU. This allows it to be accessed during the refresh cycle when the screen is being drawn, a technique used for high resolution graphics.



The ROM is wired for the selected 8K block. ROMs larger than 8K can be used with multiple banks being selected by jumpers on the ROM A13,A14 and A15 pins. In most cases, these can be all set high.



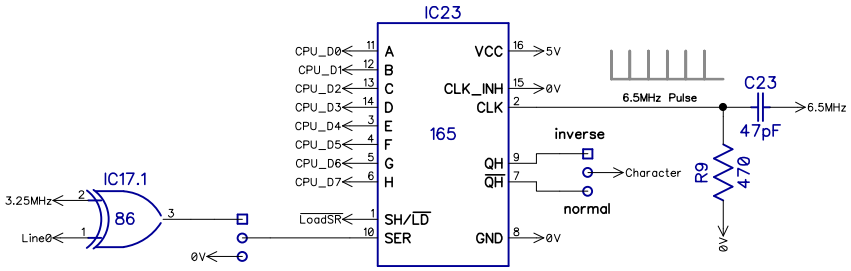
The memory map this creates is as follows, the 8K ROM, mirrored in the upper address space, and 32K RAM with the mirror at the top of RAM used for the display file.

Address Range	Use
0000-1FFF	ROM
2000-3FFF	RAM
4000-5FFF	RAM
6000-7FFF	RAM
8000-9FFF	RAM
A000-BFFF	ROM
C000-DFFF	RAM (during M1)
E000-FFFF	RAM (during M1)

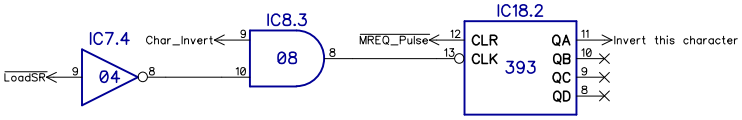
16K of this is available to BASIC, and located where the normal 16K RAM pack would be, where most software would expect it (4000-7FFF).

VIDEO

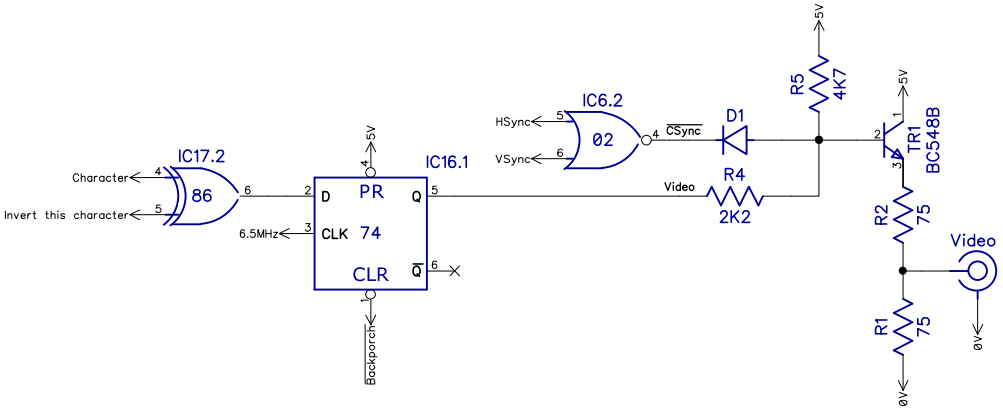
When character data has been loaded into the shift register, it is clocked out using the 6.5Mhz clock. The normal / inverse jumper selects the inverted or non-inverted output. Character data has a 1 for a pixel, 0 for a space. Black on white text requires the inverse of that, so the inverted signal is the normal one. During periods when no data has been loaded, the serial input is passed to the output. This can be selected to be 0V, which will give the background colour (normally white). When the jumper is in the other position, a signal is fed through which creates a greyscale crosshatch pattern border to the screen. This is generated from the 3.25Mhz clock which gives alternate pixels, and is XORed with the lowest bit of the line counter, so this it alternates each line. During development this was referred to as 'The mists of time'. The plan was to use this to generate a valid video signal during fast mode when a signal is not normally present, but that has not been possible.



Characters can be inverted by setting bit 7 of the character code. This is latched at the same time as the data is latched into the shift register. During optimisation, this has been implemented using some left over gates, hence the slightly unusual design. A counter is used, if the invert signal is set, there will be a single pulse which will set the output high. Each memory request cycle, the counter will be reset.



The invert signal is XORed with the character data from the shift register. In order to ensure evenly sized pixels, this is clocked through a flip flop by the 6.5MHz clock. The clear input on the flip flop is used to inject a backporch signal into the video output in order to set the black level before the actual line data starts. This video signal is mixed with the composite sync, and then buffered to provide the composite video output.



POWER

A 9V DC input is regulated down to 5V and decoupled by probably far too many decoupling capacitors. Polarity of the input is set by two jumpers to allow centre positive or centre negative supplies.