# SPI RAM 4Mb Datasheet (Rev. 1)

The SPI RAM 4Mb module is a RAM expansion module with a 1x6 PMOD style 0.1" male pin header. The module contains a single IS62WVS5128FBLL-20 SRAM chip. The chip is arranged as two stacked 2Mbit dies.

On board components provide power supply capacitor and pullup resistor on chip select.

Complete details for the memory chip and its features can be obtained from the manufacturer's datasheet:

http://www.issi.com/WW/pdf/IS62-65WVS5128FALL-BLL.pdf
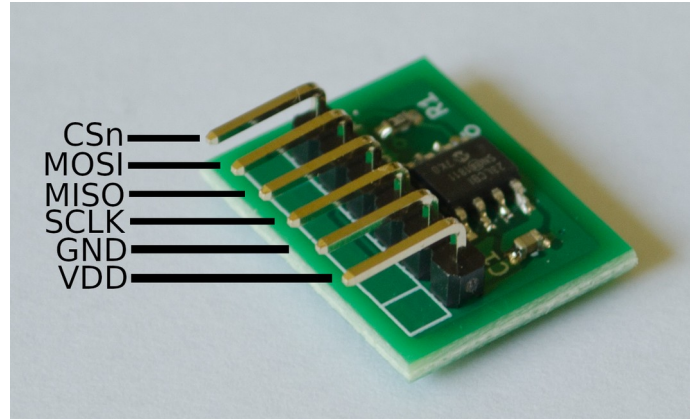
Features Overview

- Total Memory: 4 Mbit organized as 512K x 8-bit
- Max SCLK Frequency: 20 MHz
- 6-pin PMOD compatible pinout
- $\overline{CS}$ pullup 10K resistor
- 100n power decoupling capacitor
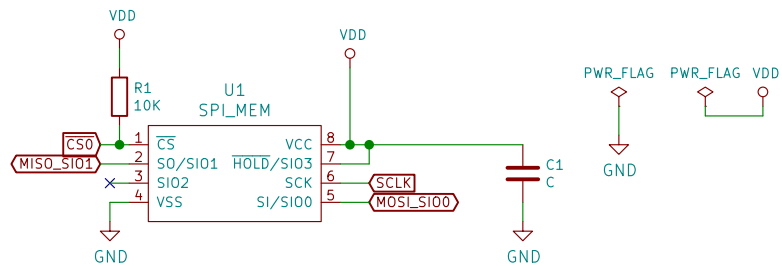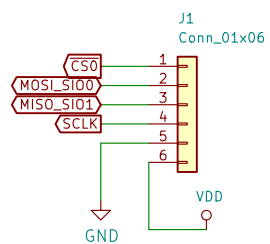- byte or page operation. See manufacturer datasheet.

Pinout

Pin Number	Name	Function
1	$\overline{CS}$	Active-low chip select
2	MOSI	Master output, Slave input.
3	MISO	Master input, Slave output
4	SCLK	Serial clock input pin.
5	GND	Ground
6	VDD	Power, 2.5V to 3.3V.

IMPORTANT!!!

***If combining multiple devices on a single SPI bus, to avoid bus contention ensure only one device's $\overline{CS}$ pin is low at any time. All others should be driven high.**

***The device is stacked with 2-die, so it has a restriction in sequential operation: The address counter cannot cross the die boundary.**

When the Address Pointer reaches the highest address of first die (3FFFFh), the address counter cannot cross to first address of 2nd die (40000h). Instead, it rolls over to (00000h). So the sequential operation must be terminated at the last address of first die (Die 0) by CS# HIGH, and begin new sequential operation from first address (40000h) of second die (Die 1) by CS# LOW.

J1
Conn_01x06

CS0 — 1
MOSI_SIO0 — 2
MISO_SIO1 — 3
SCLK — 4
5
6

GND

VDD

VDD

R1
10K

U1
SPI_MEM

CS0 — 1 CS VCC 8
MISO_SIO1 — 2 SO/SIO1 HOLD/SIO3 7
3 SIO2 SCK 6 SCLK
4 VSS SI/SIO0 5 MOSI_SIO0

GND

VDD

C1
C

GND

PWR_FLAG   PWR_FLAG VDD

GND